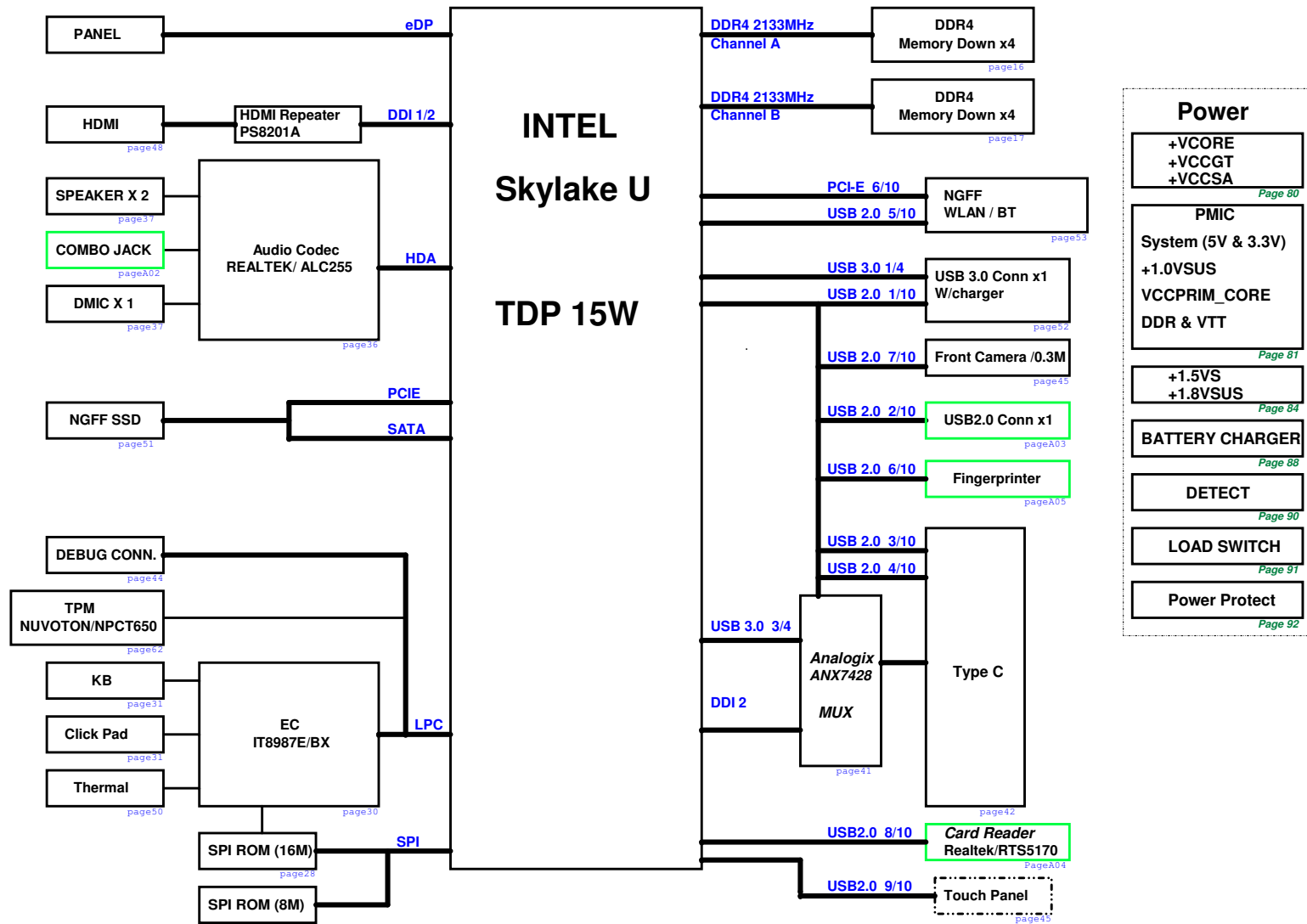


14" Cassiopeia (X3) for Skylake U Platform Block Diagram



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Discharge Circuit

Page 57

DC & BATT. Conn.

Page 60

Reset Circuit

Page 32

Skew Holes

Page 65

<Variant Name>

PEGATRON Title : Block Diagram

PEGATRON PROPRIETARY AND CONFIDENTIAL

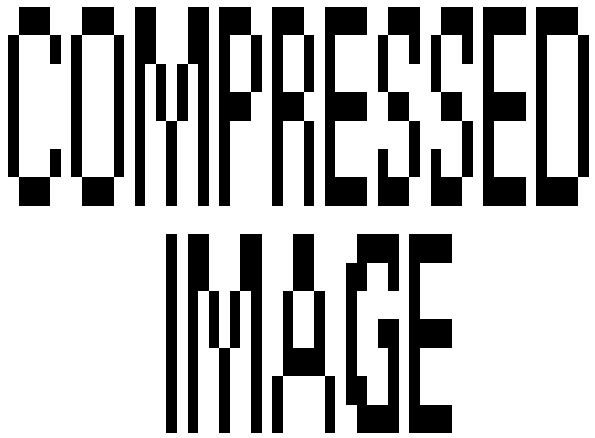
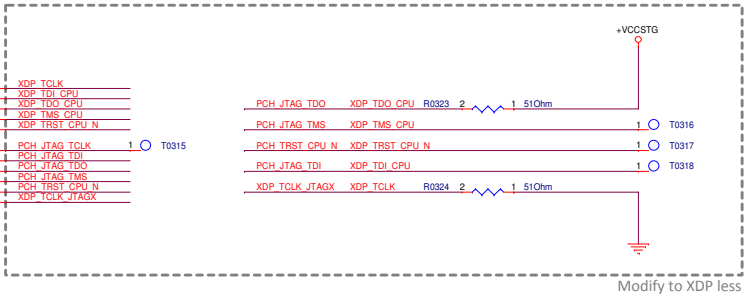
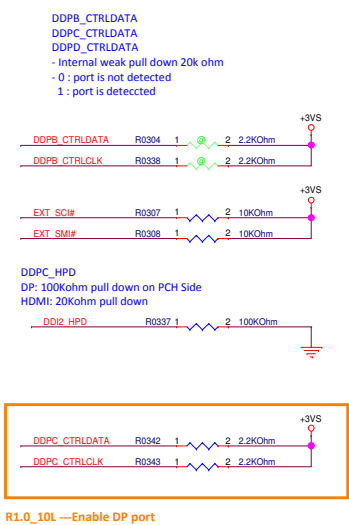
BG1HW3

Engineer: Andy Kao

Size Project Name Custom X3 Rev 1.0

Date: Monday, July 11, 2016 Sheet 1 of 97

5			4			3			2			1														
EC GPIO			Use As			Signal Name			EC GPIO			Use As			Signal Name			EC GPIO			Use As			Signal Name		

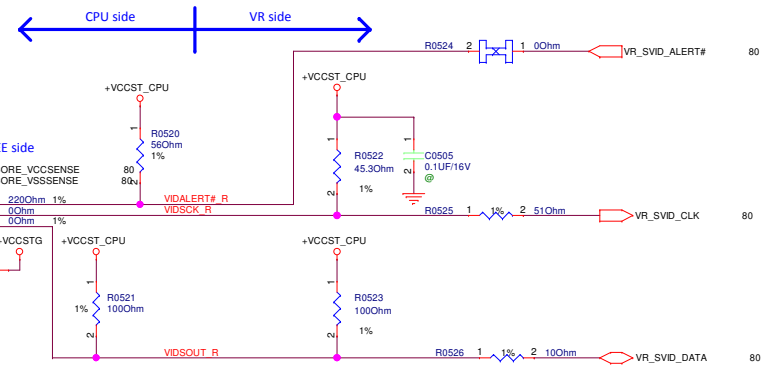


SKL 2+2, +V1.8VS_EDRAM / +V_EDRAM_VR / +V_EOPIO_VR
From Intel, SKL-U 2+2 reserve these pins PD to GND

RSVD NC

29A

+V CORE +V CORE 80
+VCCSTG +VCCSTG 3,7
+VCCST_CPU +VCCST_CPU 3,7,9,25,32



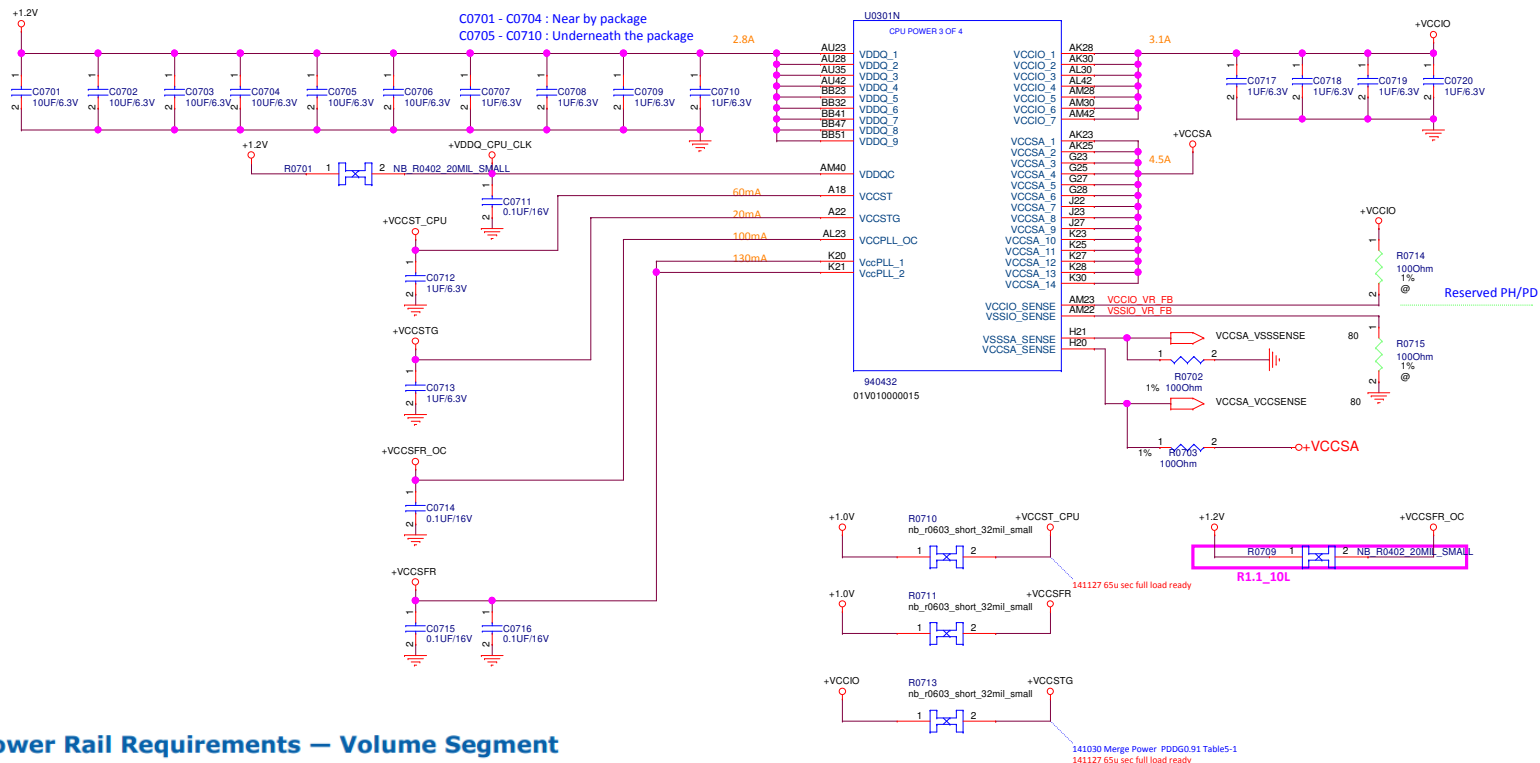
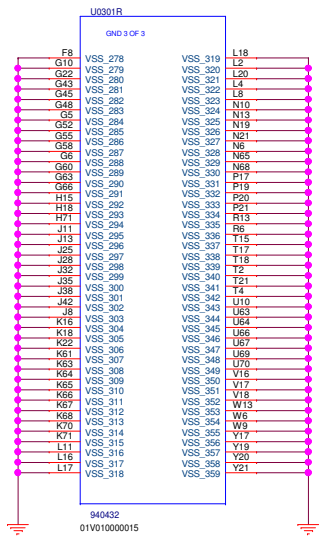
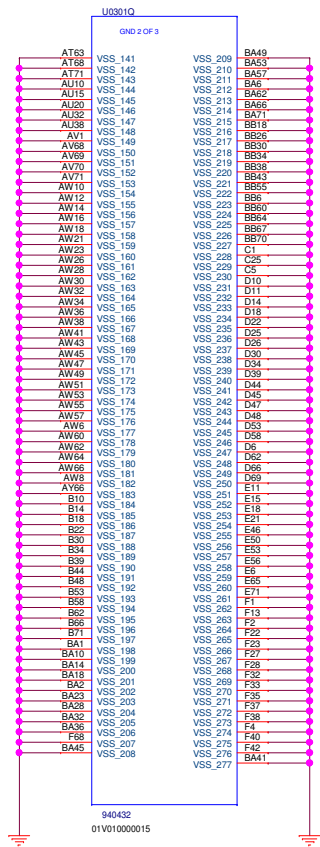
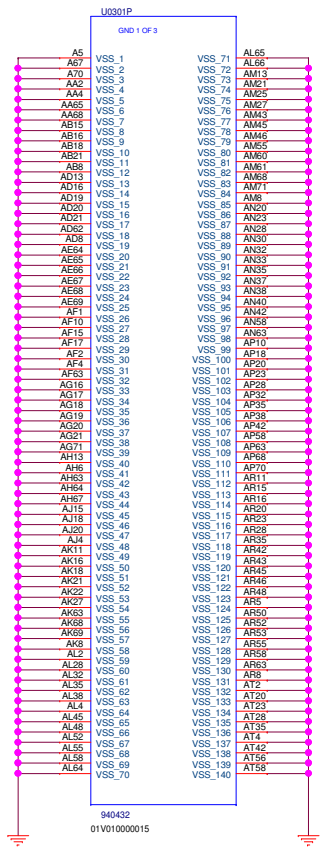
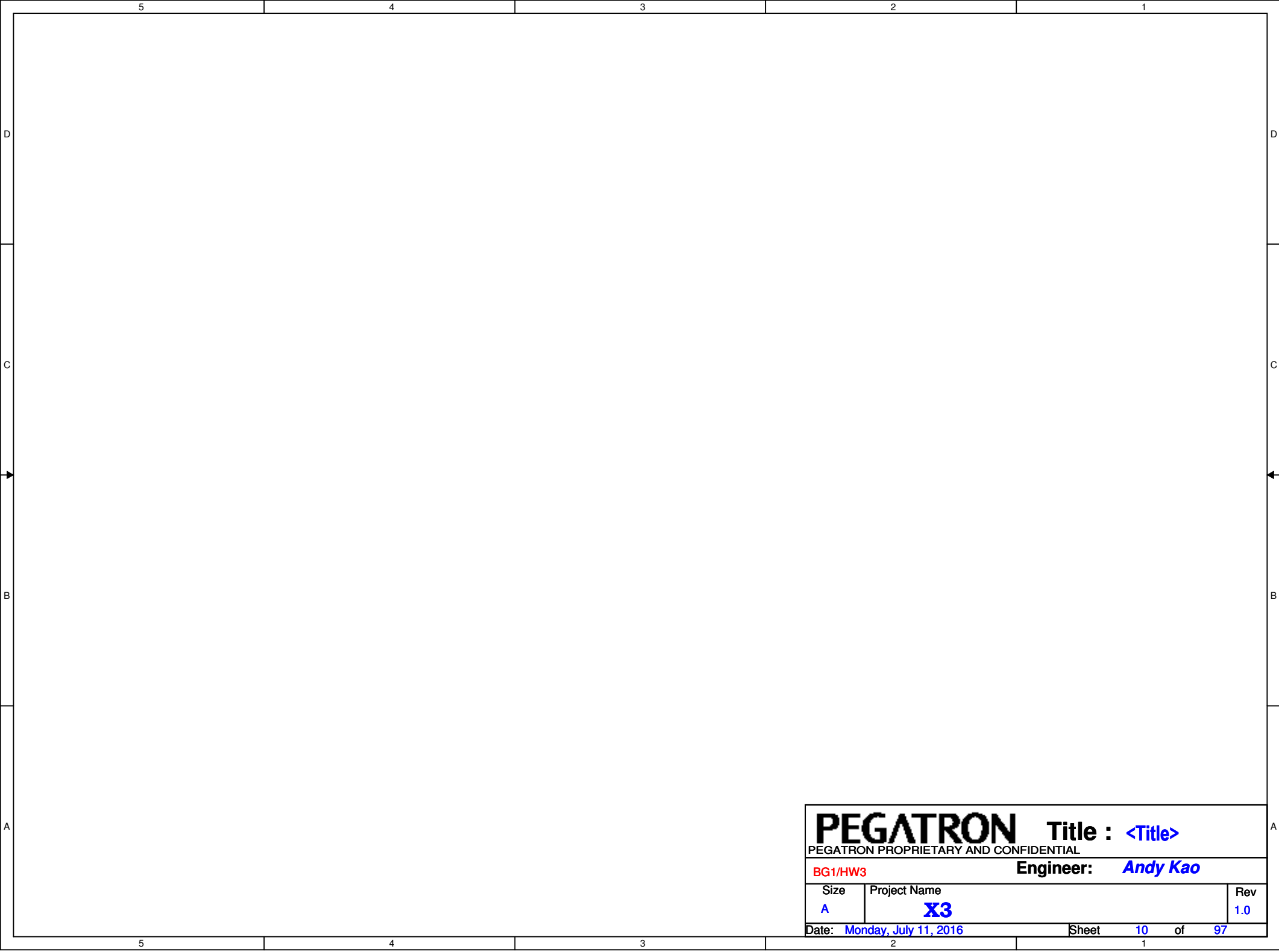


Table 5-1. Power Rail Requirements — Volume Segment — U-Line

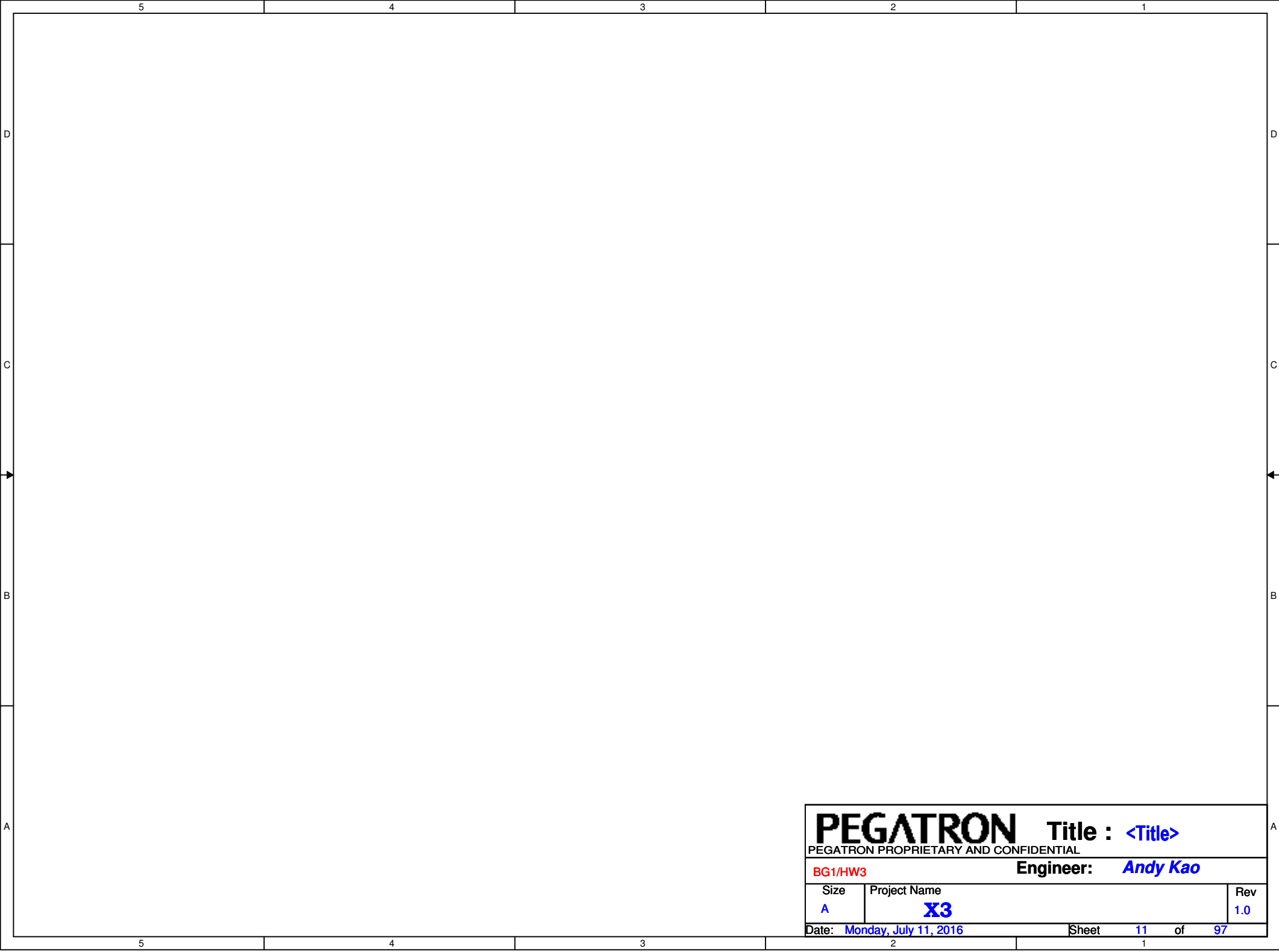
Load switch (LS)	LS ENABLE	Load/Rail name	I _{max} (A)
<= 65usec full load ready (Note 16)	SLP_S4#	Vcc _{ST}	0.04
		Vcc _{PLL} (Vcc _{SFR})	0.12
<= 65usec full load ready	SLP_S3# AND SLP_S0#	Vcc _{IO}	3.0
		Vcc _{STG}	0.04

16. VCCST ramp time can potentially be slowed than listed, depending on platform design. However, all timings documented in the PSS chapter must be met, specifically T_{cpu_04}

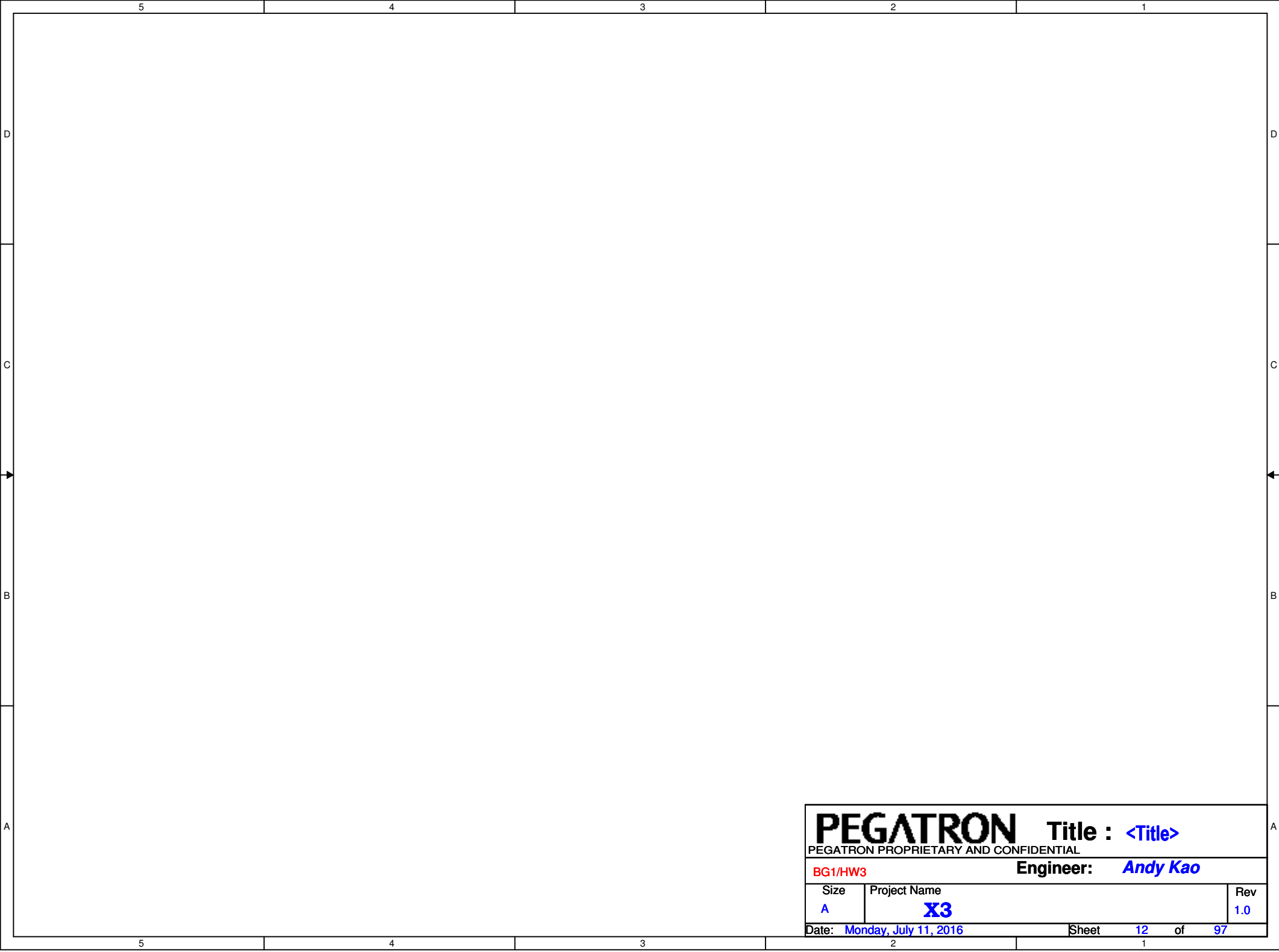




PEGATRON		Title : <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size <i>A</i>	Project Name X3		Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>10</i> of <i>97</i>	

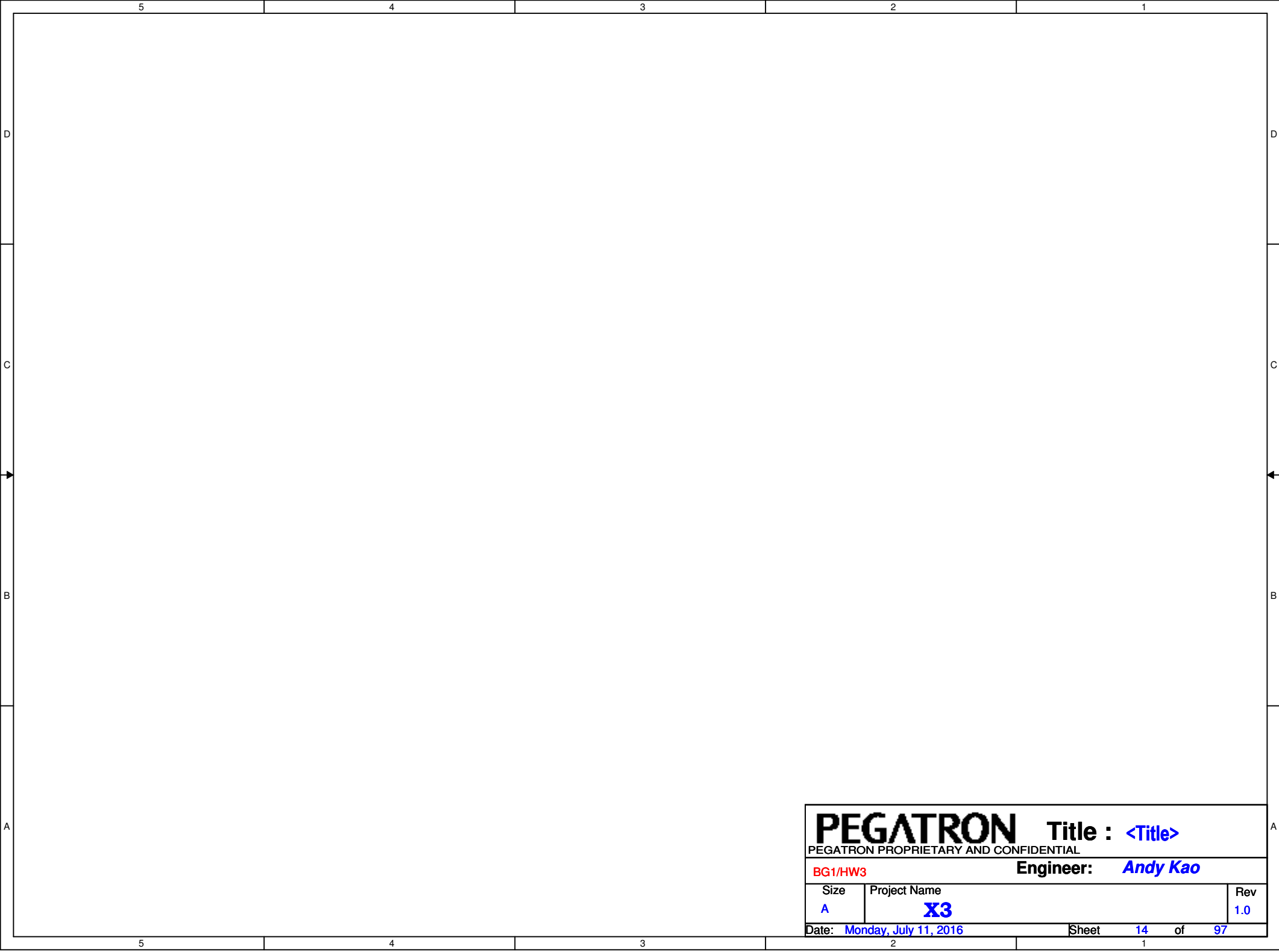


PEGATRON Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: <i>Andy Kao</i>
Size A	Project Name X3	Rev 1.0
Date: Monday, July 11, 2016		Sheet 11 of 97





PEGATRON		Title : <Title>	
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Size <i>A</i>	Project Name X3		Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>12</i> of <i>97</i>	

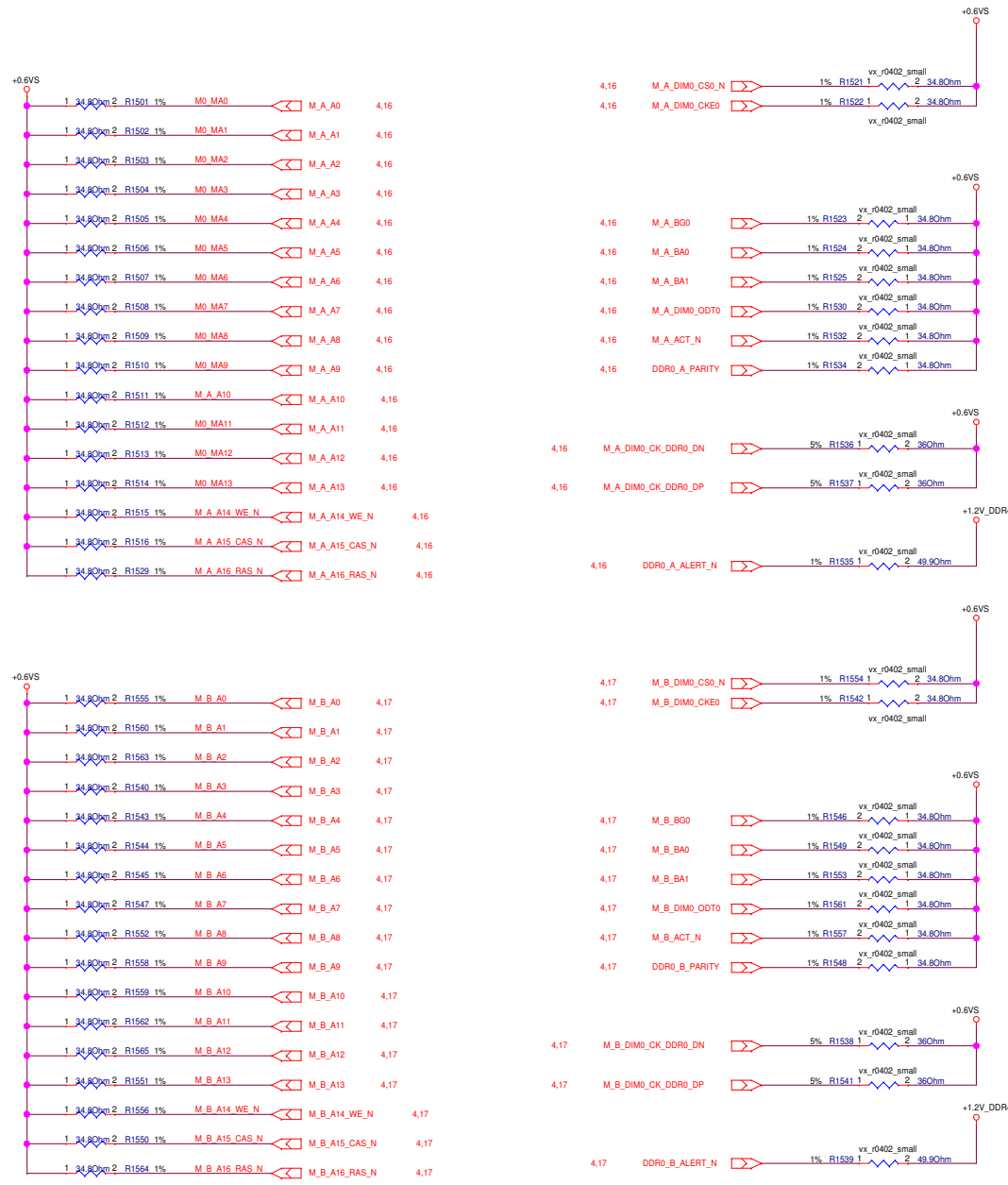
5					4					3					2					1																																																																																														
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B																																																																																																																		
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										<table><tr><td colspan="10">PEGATRON</td><td colspan="5">Title : <Title></td></tr><tr><td colspan="15">PEGATRON PROPRIETARY AND CONFIDENTIAL</td></tr><tr><td colspan="10">BG1/HW3</td><td colspan="5">Engineer: Andy Kao</td></tr><tr><td colspan="2">Size</td><td colspan="10">Project Name</td><td colspan="3">Rev</td></tr><tr><td colspan="2">A</td><td colspan="10">X3</td><td colspan="3">1.0</td></tr><tr><td colspan="10">Date: Monday, July 11, 2016</td><td colspan="5">Sheet 13 of 97</td></tr></table>															PEGATRON										Title : <Title>					PEGATRON PROPRIETARY AND CONFIDENTIAL															BG1/HW3										Engineer: Andy Kao					Size		Project Name										Rev			A		X3										1.0			Date: Monday, July 11, 2016										Sheet 13 of 97				
PEGATRON										Title : <Title>																																																																																																								
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Date: Monday, July 11, 2016										Sheet 13 of 97																																																																																																								
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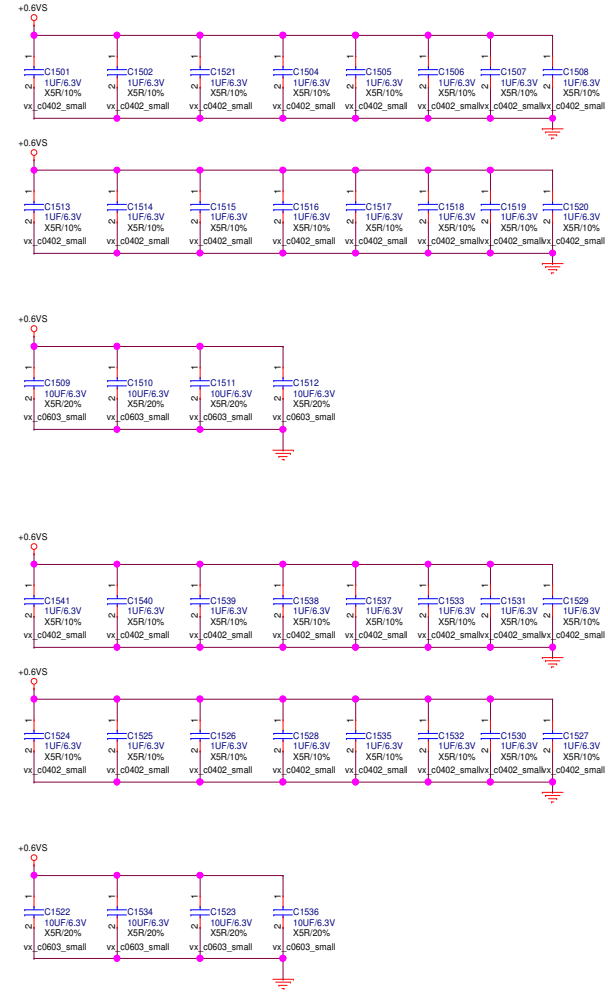
PEGATRON		Title : <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size <i>A</i>	Project Name X3		Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>14</i> of <i>97</i>	

DDR4(0)_Termination

+0.6VS  +0.6VS 57,83
+1.2V_DDR4  +1.2V_DDR4 4,7,16,17,19,57,83

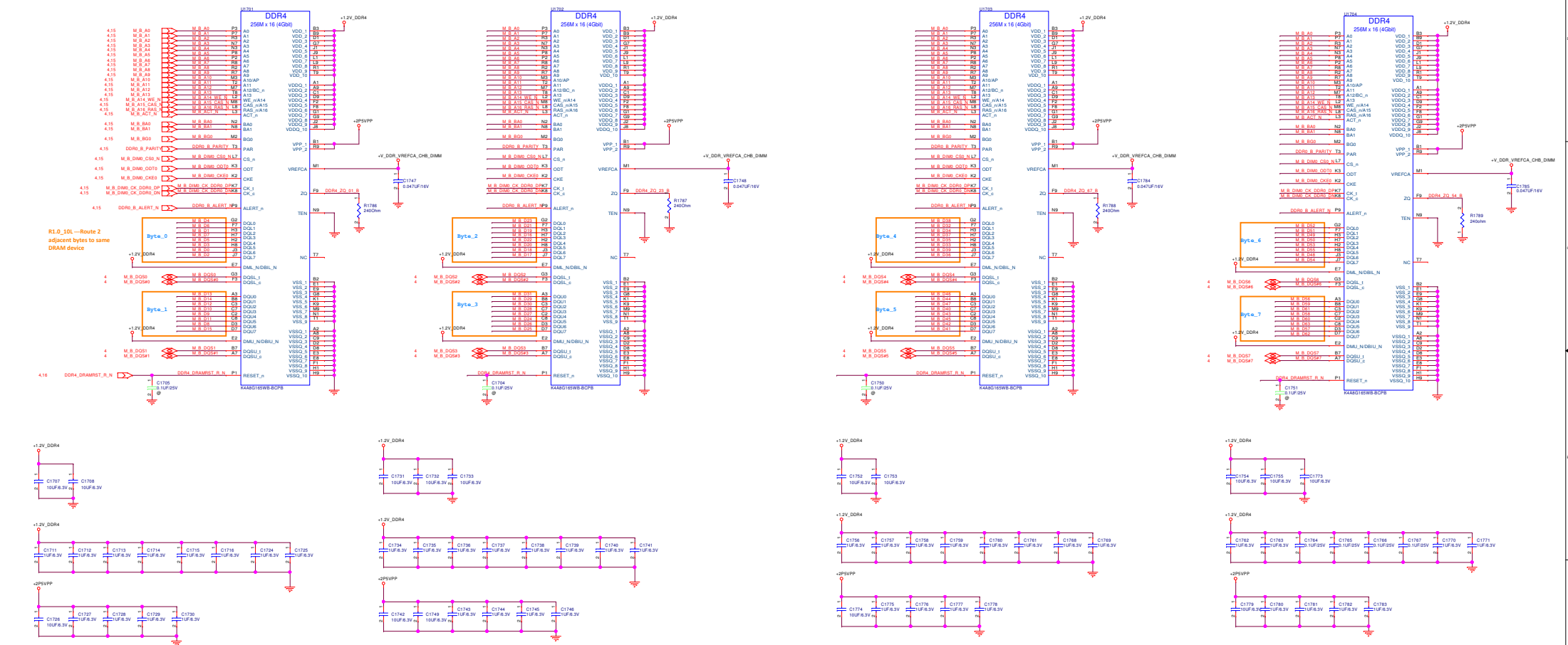


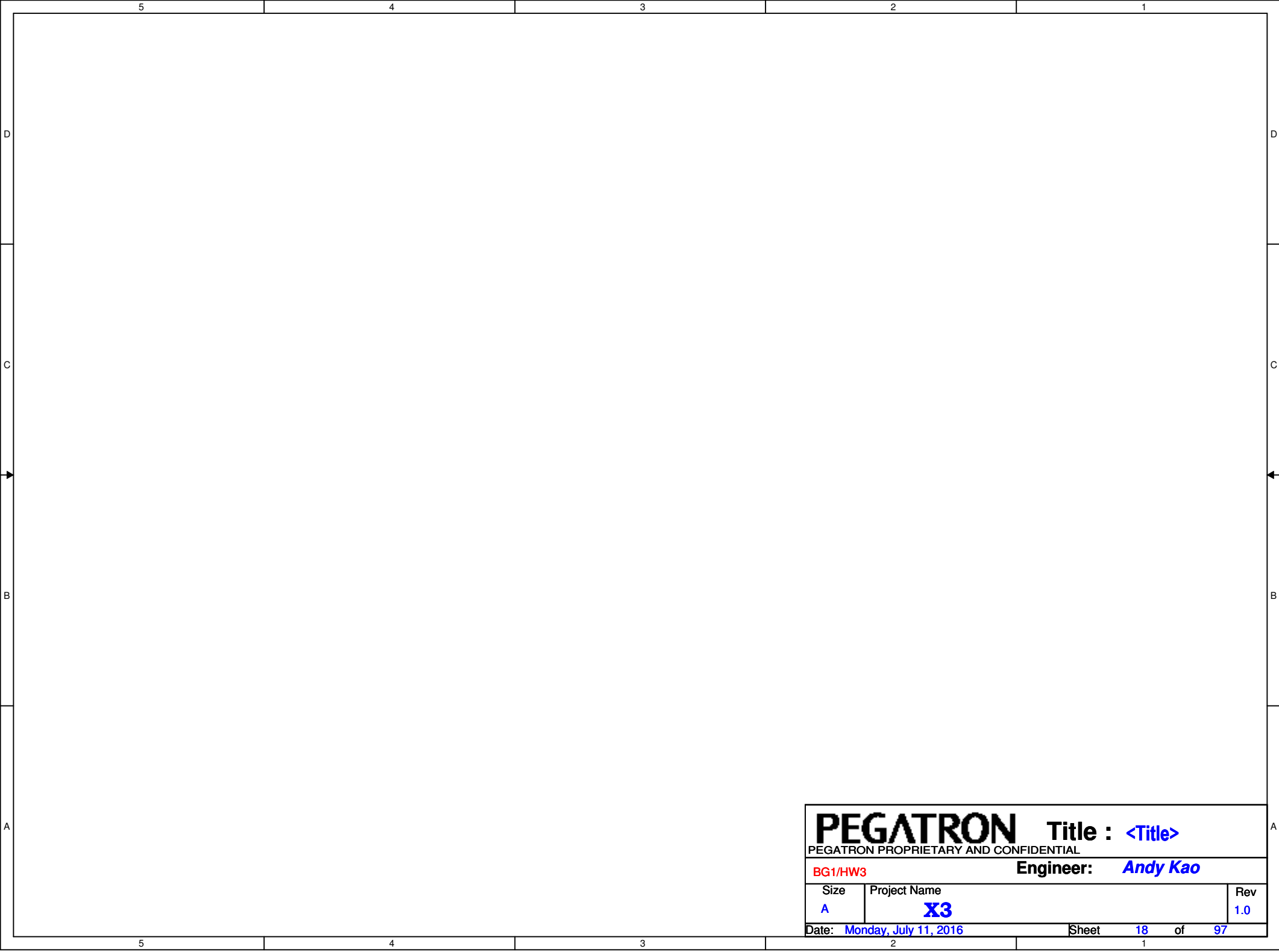
Average placed close to +VDDQ_VTT power plane





DDR4(2)_CH1

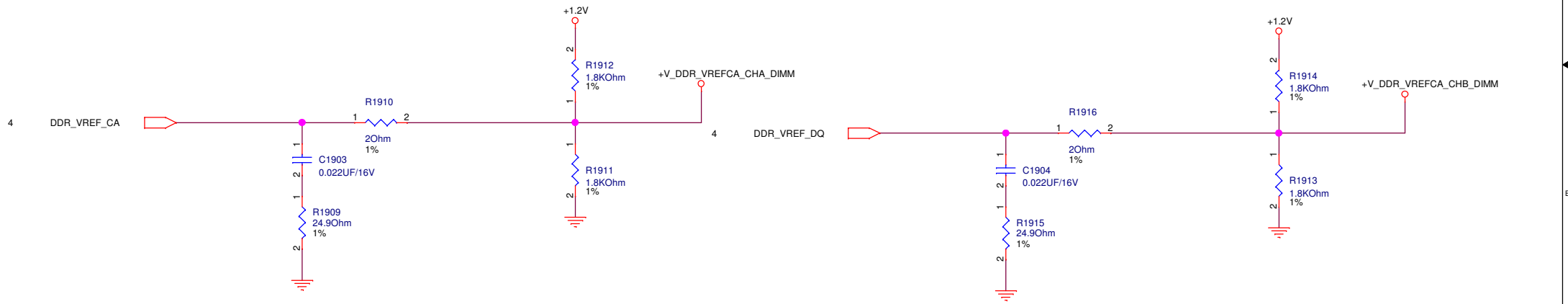




PEGATRON Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
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Size A	Project Name X3	Rev 1.0
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+1.2V		+1.2V	4,7,15,16,17,57,83
+V_DDR_VREFCA_CHB_DIMM		+V_DDR_VREFCA_CHB_DIMM	17
+V_DDR_VREFCA_CHA_DIMM		+V_DDR_VREFCA_CHA_DIMM	16

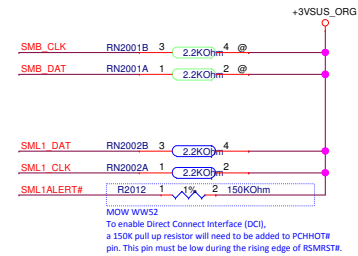
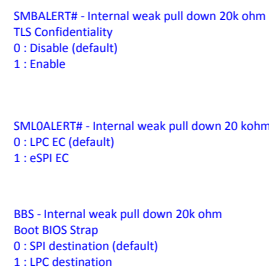
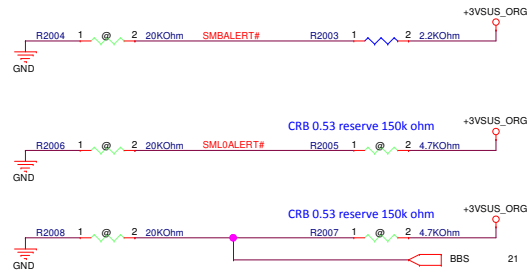
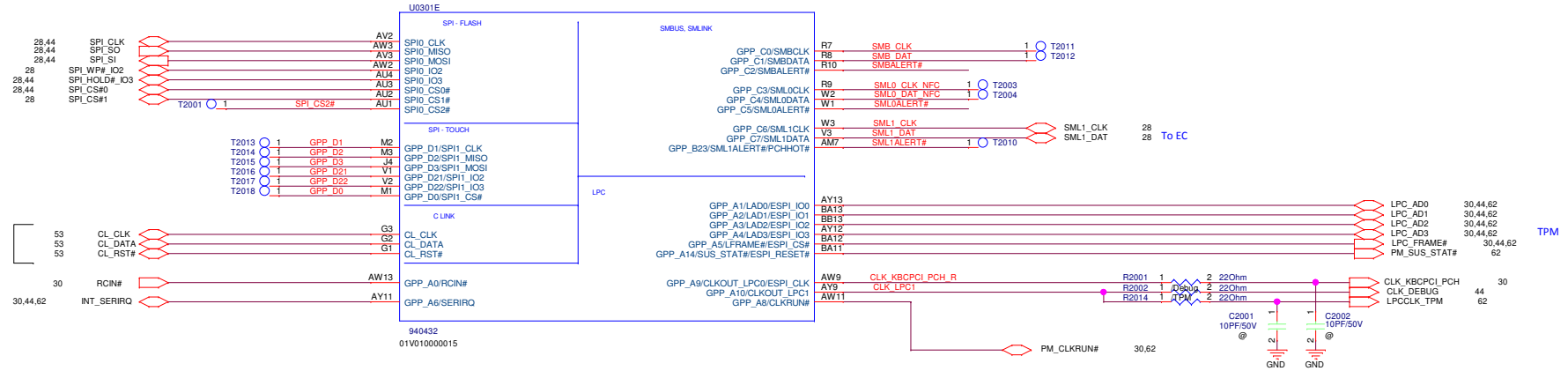
DDR4 Vref (Intel Schematic Review)



<Variant Name>		
PEGATRON Title : DDR3(3)_CA/DQ Voltage		
BG1/HW3 Engineer: Andy Kao		
Size B	Project Name X3	Rev 1.0
Date: Monday, July 11, 2016 Sheet 19 of 97		

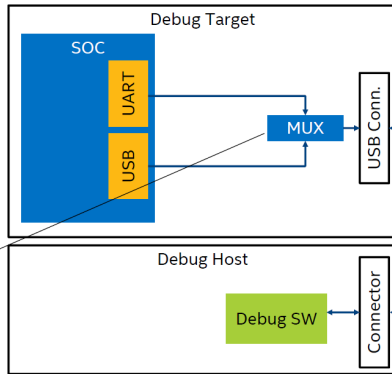
ME
BIOS+EC_PBA

WLAN/BT

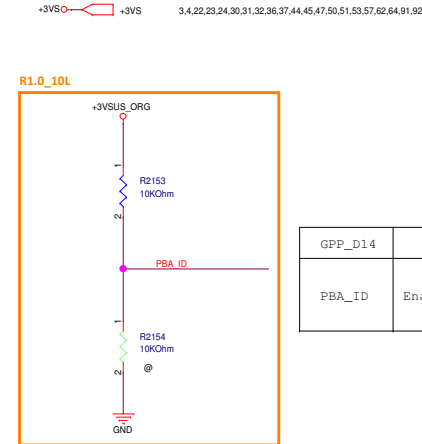


Microsoft® Windows® 7 System WHCK Requirement – OEM platforms are required to include a supported OS debug interface, accessible by an enduser. This allows developers to help in driver debug. The supported Windows 7 debug interfaces are EHCI, 1394 port and COM port. With skylake EHCI Removal, Potential Gap with Windows® 7 Kernel Debug and OS Installation – Mitigation Required

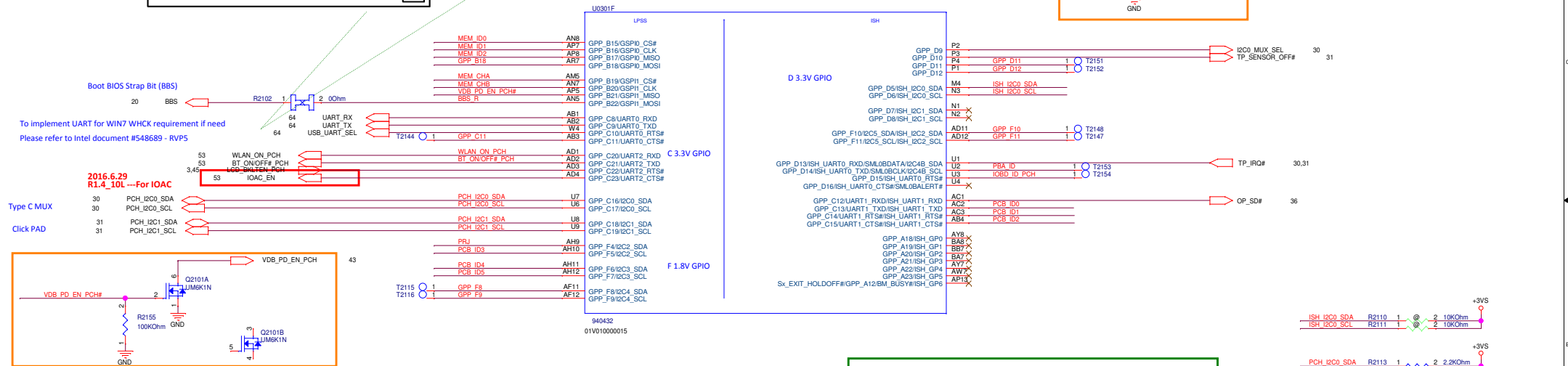
COMPRESSED IMAGE



MUX controlled by system BIOS

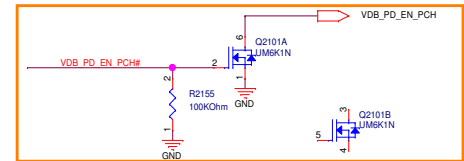


GPP_D14	1	0
PBA_ID	Enable	Disable

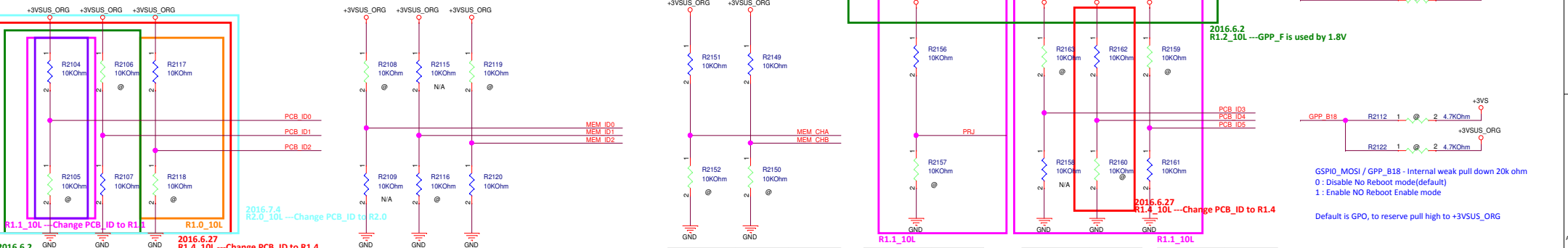


Type C MUX

Click PAD



R1.0_10L ---Follow HAWAII type-c design



2016.6.2 R1.2_10L ---Change PCB_ID to R1.2
2016.6.14 R1.3_10L ---Change PCB_ID to R1.3
2016.6.27 R1.4_10L ---Change PCB_ID to R1.4

MB Version ID

PCB_ID4 (GPP_F6)	PCB_ID1 (GPP_C14)	PCB_ID0 (GPP_C13)	PCB_ID2 (GPP_C15)	MEM_ID1 (GPP_B16)	MEM_ID2 (GPP_B17)	MEM_ID0 (GPP_B15)
R1.0	0	0	0	8L	0	0
R1.1	0	0	1	10L	1	0
R1.2	0	1	0	8Gb	1	0
R1.3	0	1	1			
R1.4	1	0	0			
R2.0	1	0	1			

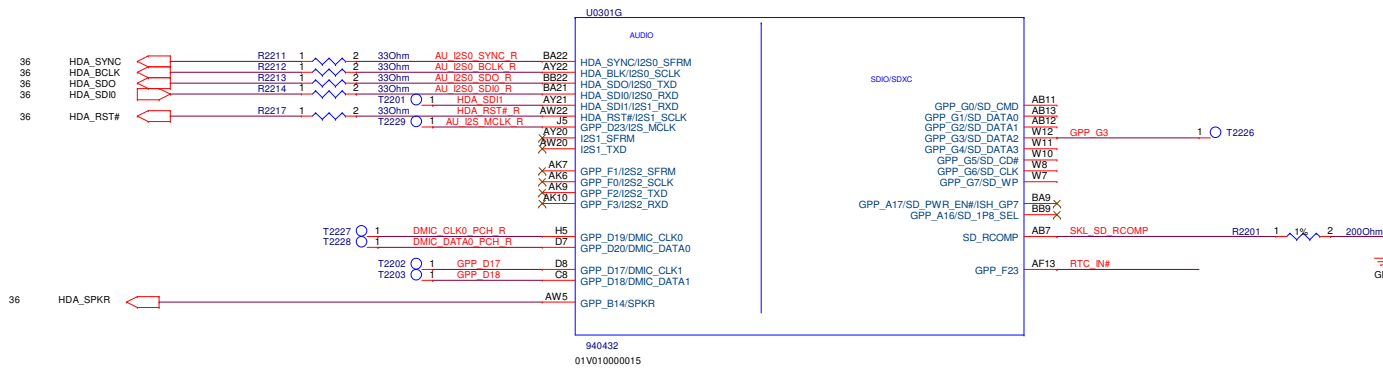
Memory ID

GPP_B19 (0)	CHA	CHB
GPP_B19 (1)	Disable	Enable
GPP_B20 (0)	Enable	Disable
GPP_B20 (1)	Enable	Enable

GPP_F4 (0)	PRJ
GPP_F4 (1)	M3

GPP_F5 (0)	PCB_ID3
GPP_F5 (1)	SKL

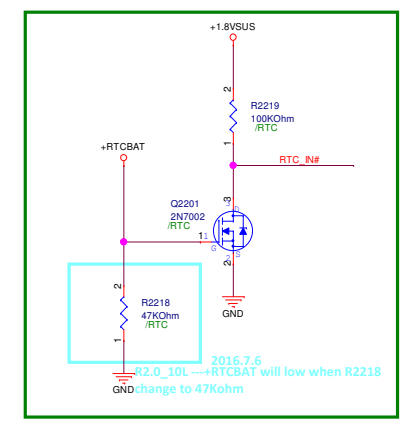
GPP_F7 (0)	PCB_ID5
GPP_F7 (1)	2133



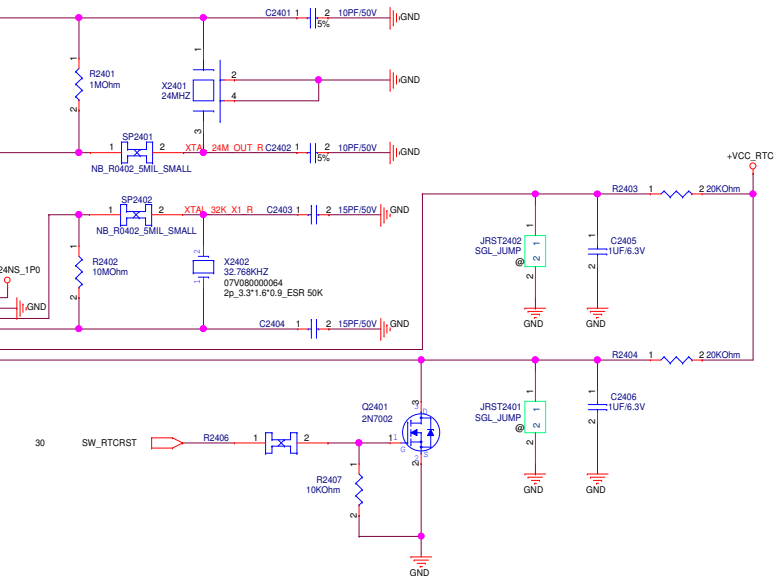
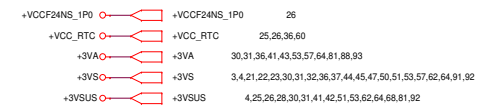
+VCCPAZIO 26
+3VS 3,4,21,23,24,30,31,32,36,37,44,45,47,50,51,53,57,62,64,91,92
+3VSUS_ORG 20,21,23,25,26

SPKR - Internal weak pull down
0 : Disable TOP Swap mode (default)
1 : Enable Top Swap Enable
Default is GPO, to reserve pull high to +3VSUS_ORG

AU_I2S0_SDO_R - Internal weak pull down
0 : Enable security measure defined in the Flash Descriptor
1 : Disable Flash Descriptor Security



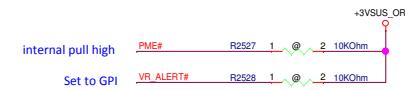
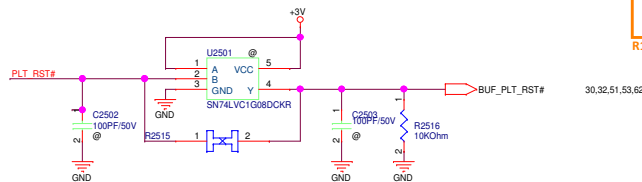
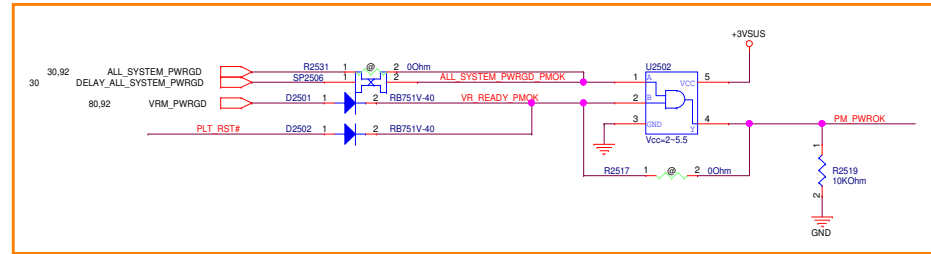
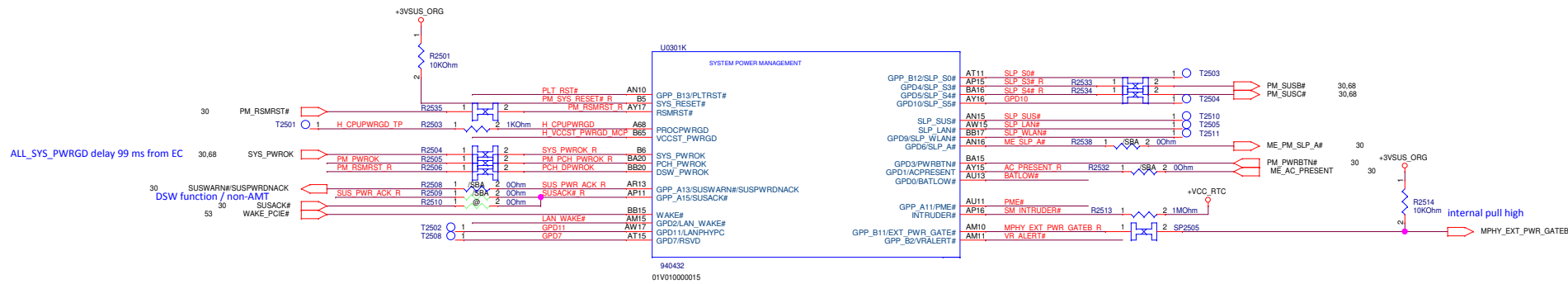
2016.5.11
R1.2_10L ---RTC detect circuit



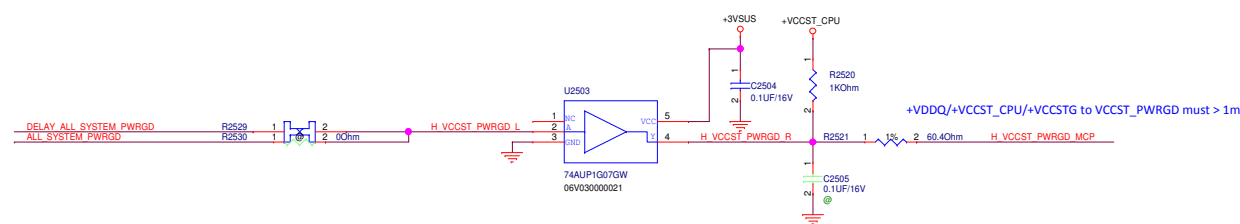
Remove SUSCLK

BG1/HW3		Engineer: Andy Kao	
Size C	Project Name X3	Rev 1.0	
Date: Monday, July 11, 2016		Sheet 24 of 97	

+3VSUS_ORG	20,21,22,23,26
+VCC_RTC	24,26,36,60
+VCCDSW	26,30
+VCCST_CPU	3,5,7,9,32
+3V	31,57,82,91
+3VSUS	4,24,26,28,30,31,41,42,51,53,62,64,68,81,92



EC delay ALL_SYSTEM_PWRGD 2ms

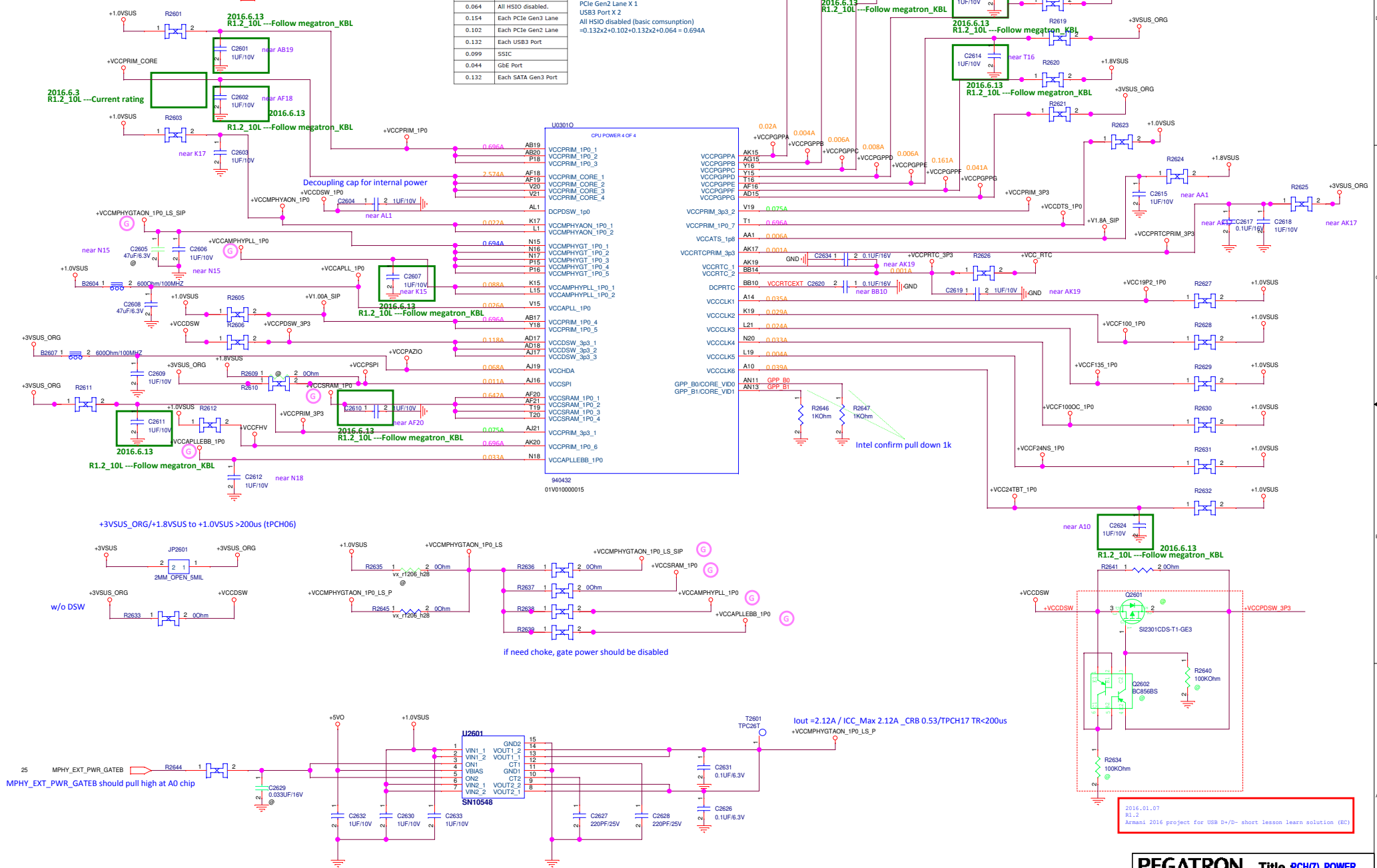


+1.0VSUS	82
+VCCDSW	25,30
+1.8VSUS	9,21,22,84
+VCCPAZIO	22
+VCC_RTC	24,25,36,60
+VCCF24NS_1P0	+VCCF24NS_1P0 24
+3VSUS_ORG	+3VSUS_ORG 20,21,22,23,25
+3VSUS	4,24,25,28,30,31,41,42,51,53,62,64,68,81,92

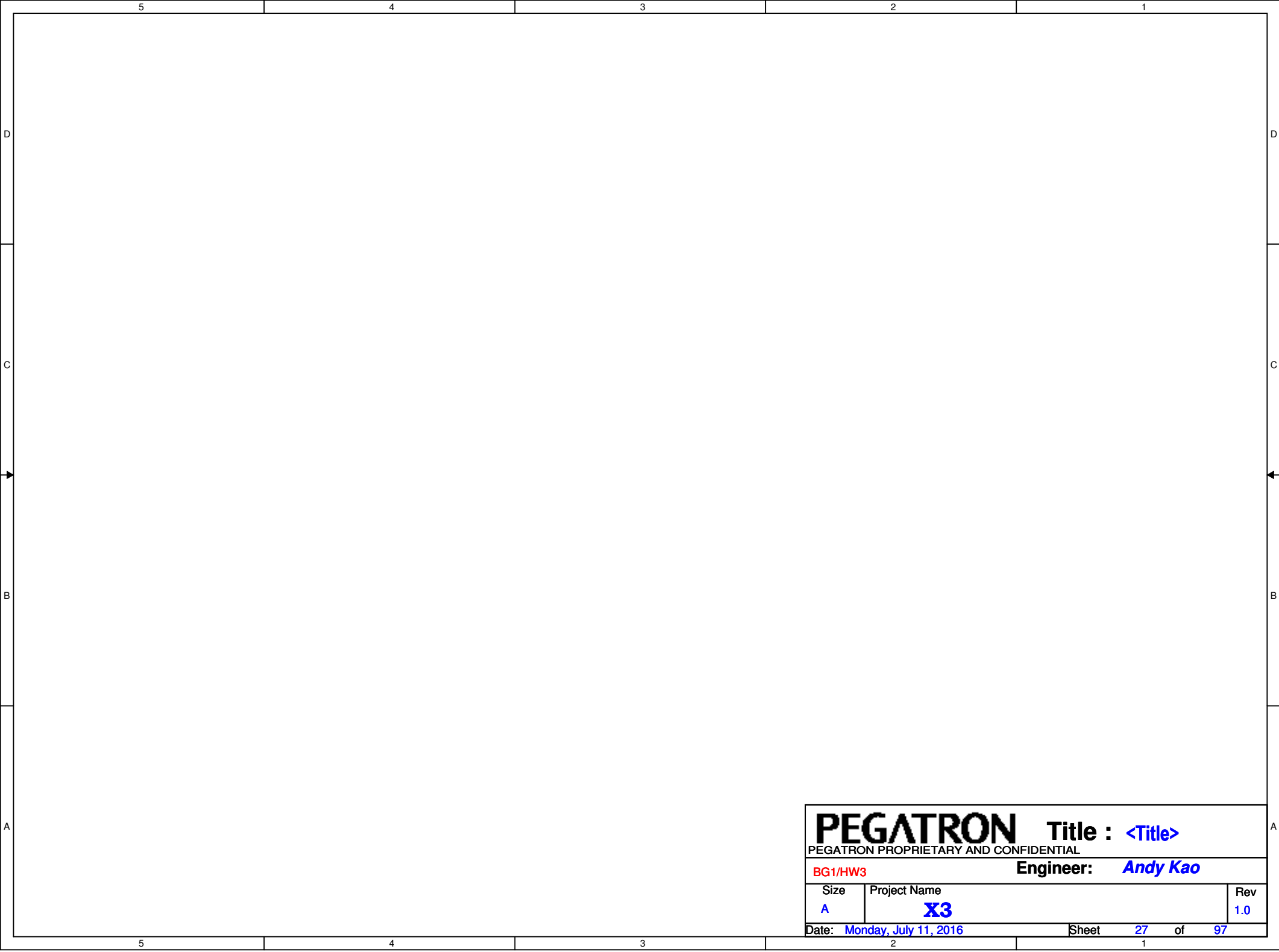
Table 10-5. SKL U / SKL Y PCH-LP
VCCMPHY_1p0 Icc Adder Per HSI0 Lane

Icc (A)	Details
0.064	All HSI0 disabled.
0.154	Each PCIe Gen3 Lane
0.102	Each PCIe Gen2 Lane
0.132	Each USB3 Port
0.099	SSIC
0.044	GBE Port
0.132	Each SATA Gen3 Port

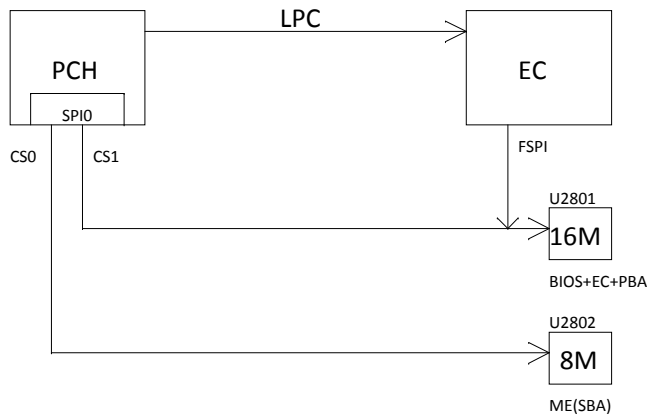
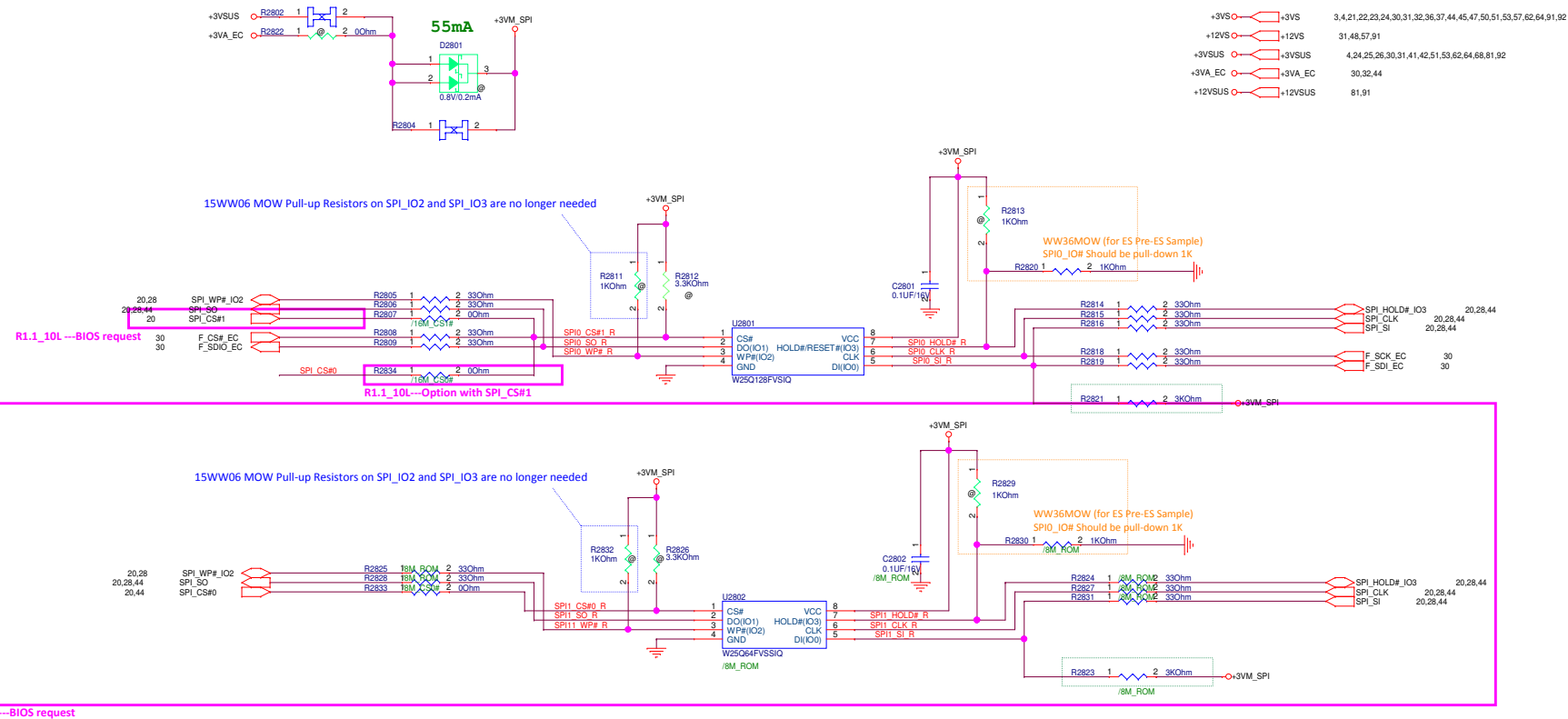
SATA Gen3 Port X2
PCIe Gen2 Lane X1
USB3 Port X2
All HSI0 disabled (basic consumption)
=0.132x2+0.102+0.132x2+0.064 = 0.694A



2016.01.07
R1.2
Armani 2016 project for USB D+/D- short lesson learn solution (EC)

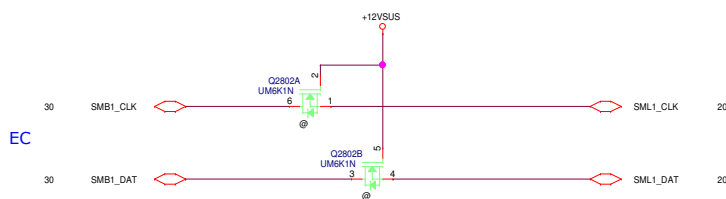


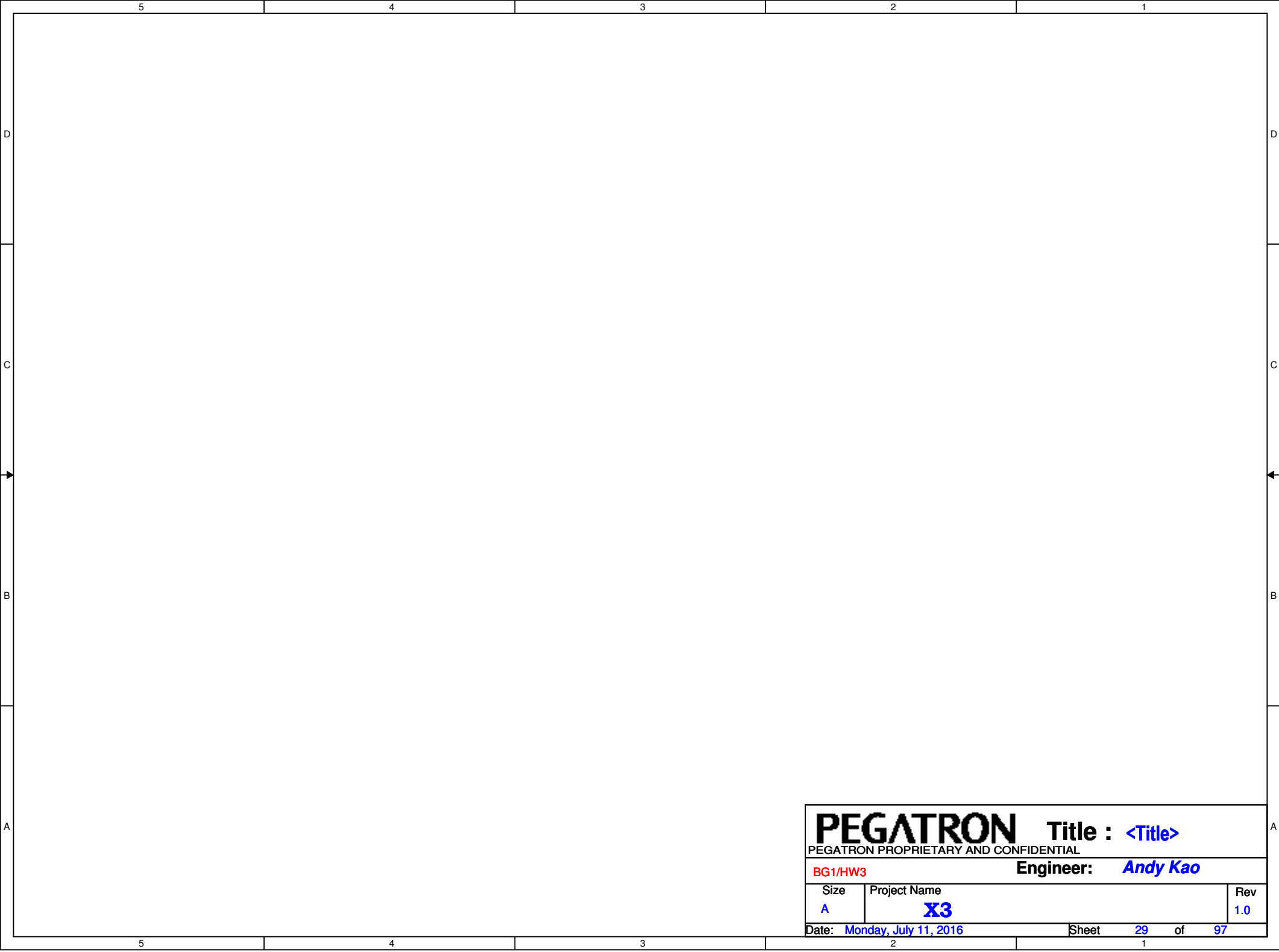
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BG1/HW3		Engineer: <i>Andy Kao</i>
Size <i>A</i>	Project Name X3	Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>27</i> of <i>97</i>



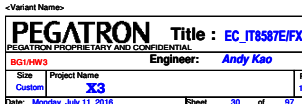
PCH SMBus

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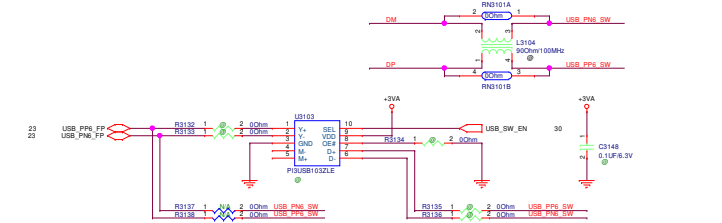
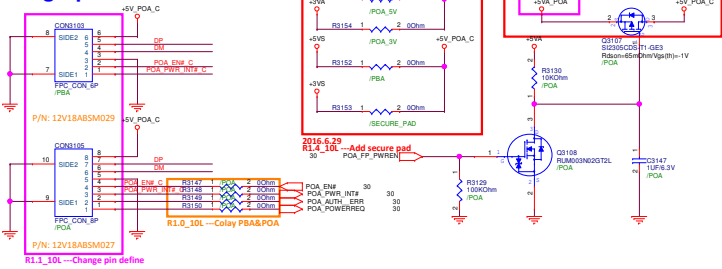




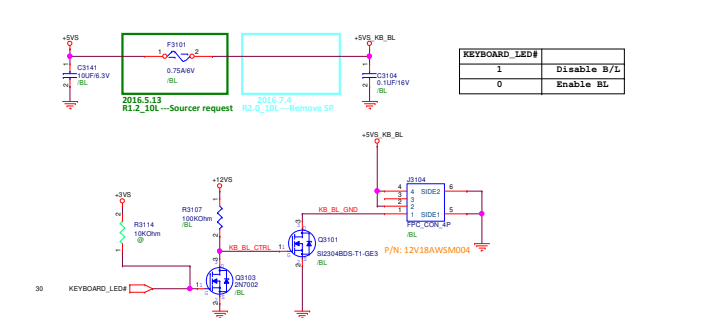
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size <i>A</i>	Project Name X3		Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>29</i> of <i>97</i>	



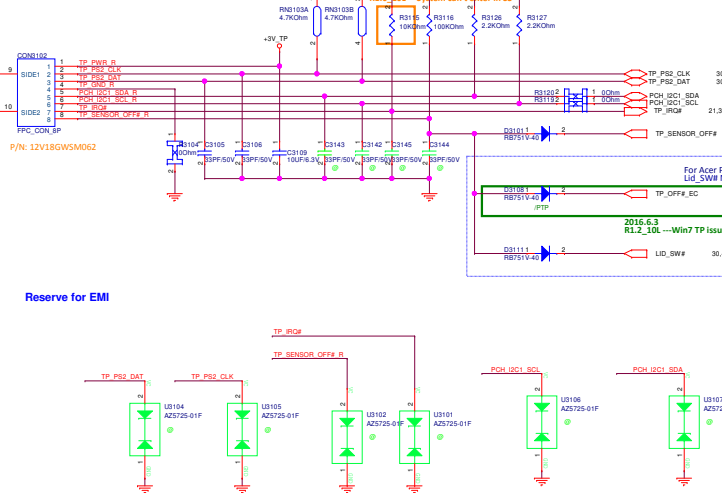
Fingerprinter



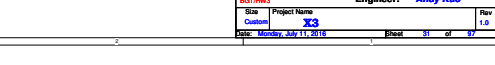
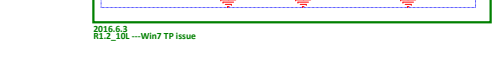
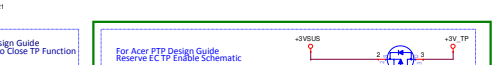
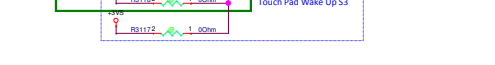
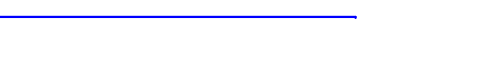
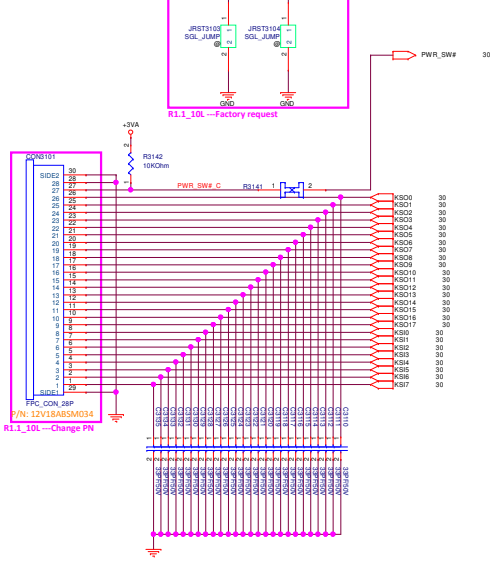
Keyboard LED

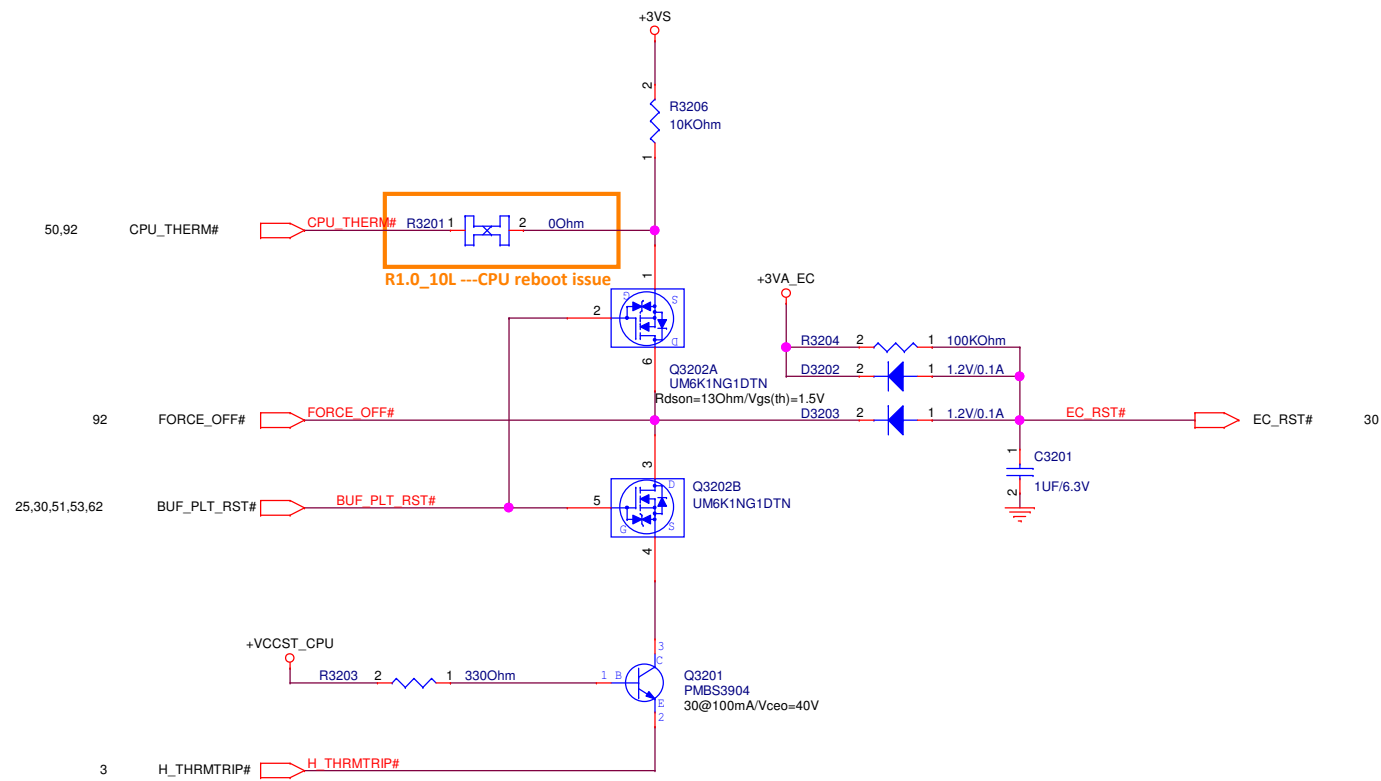


Click Pad



Keyboard



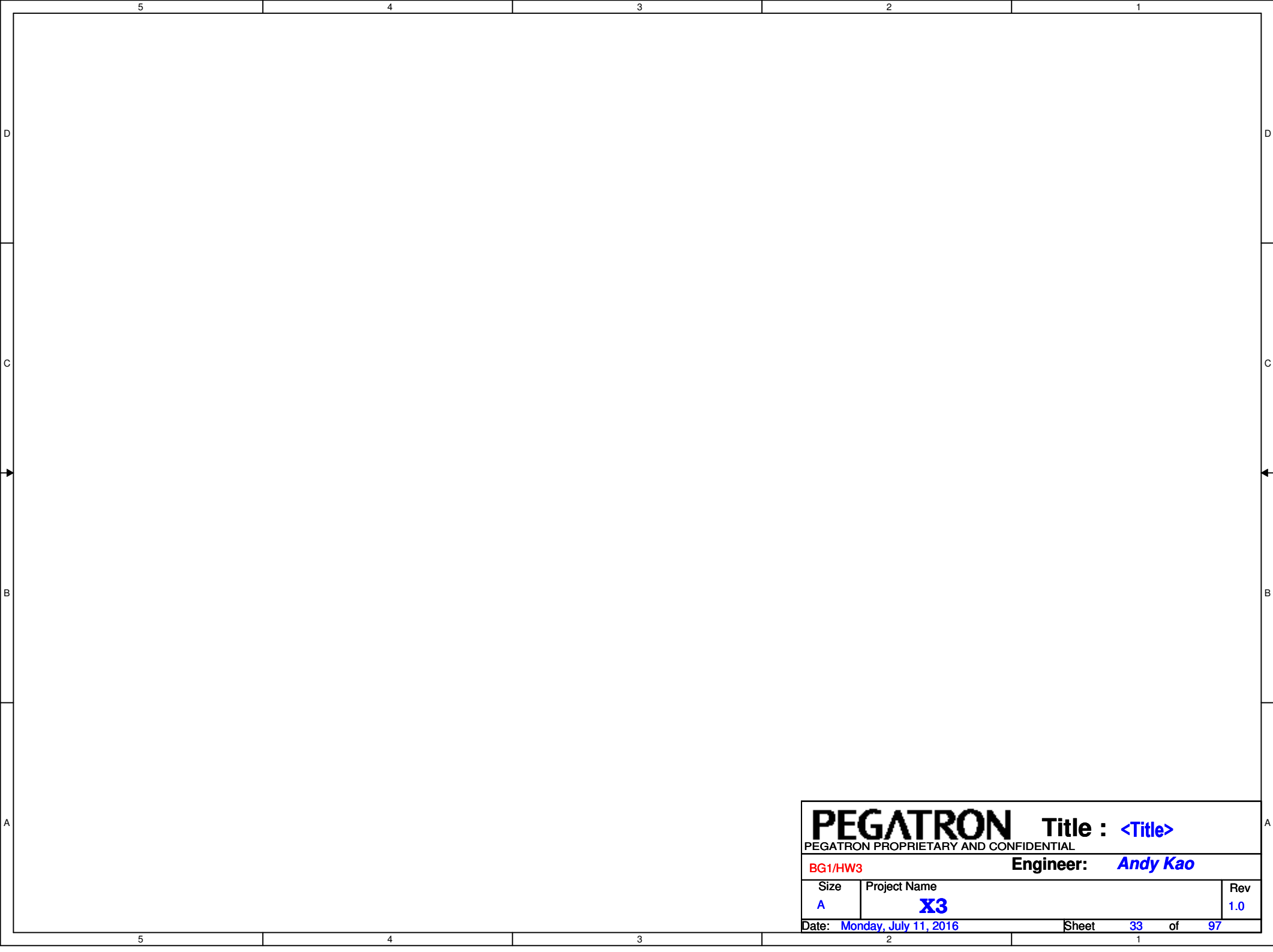


+VCCST_CPU +VCCST_CPU 3,5,7,9,25

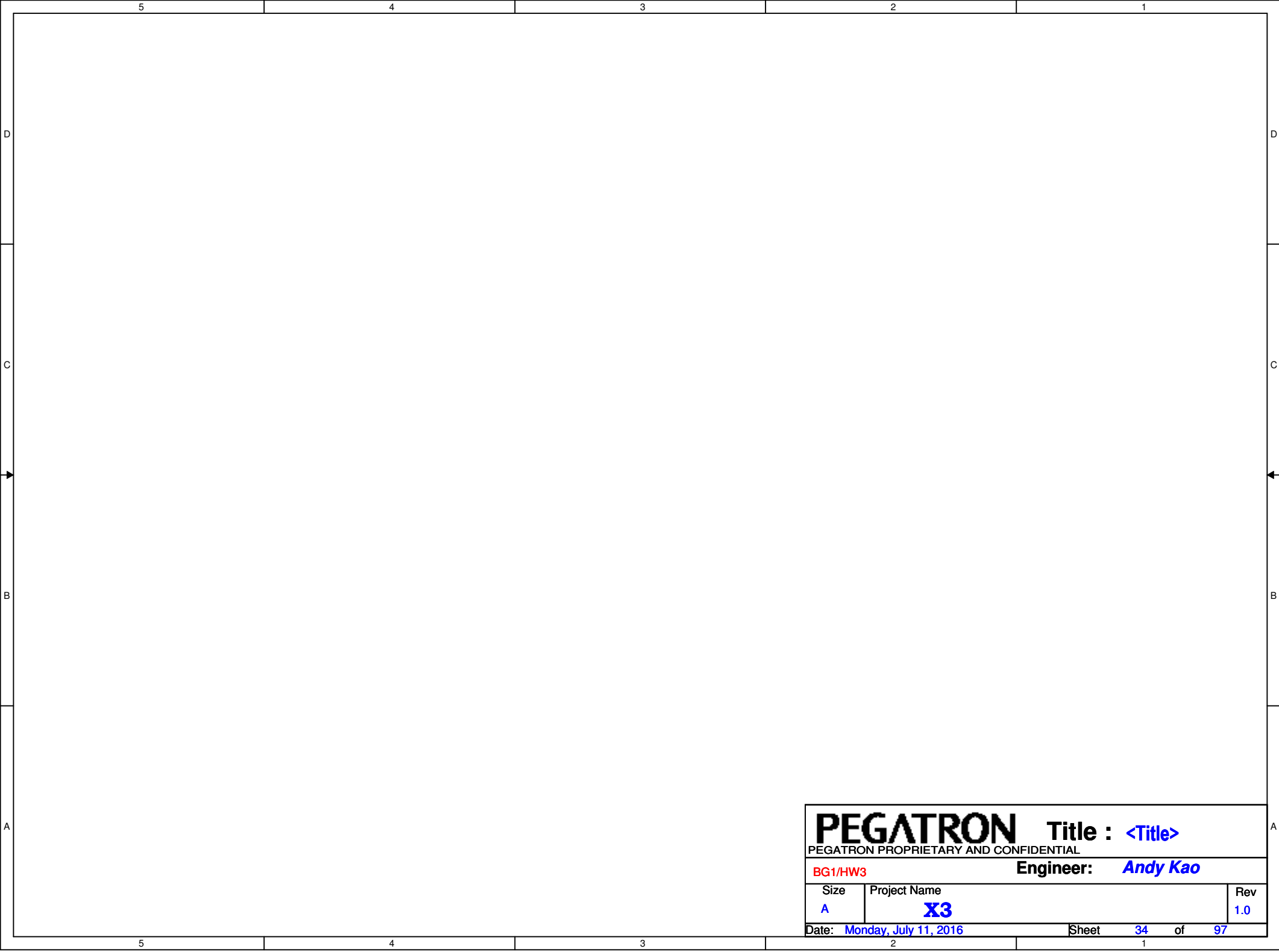
+3VA_EC +3VA_EC 28,30,44

+3VS +3VS 3,4,21,22,23,24,30,31,36,37,44,45,47,50,51,53,57,62,64,91,92

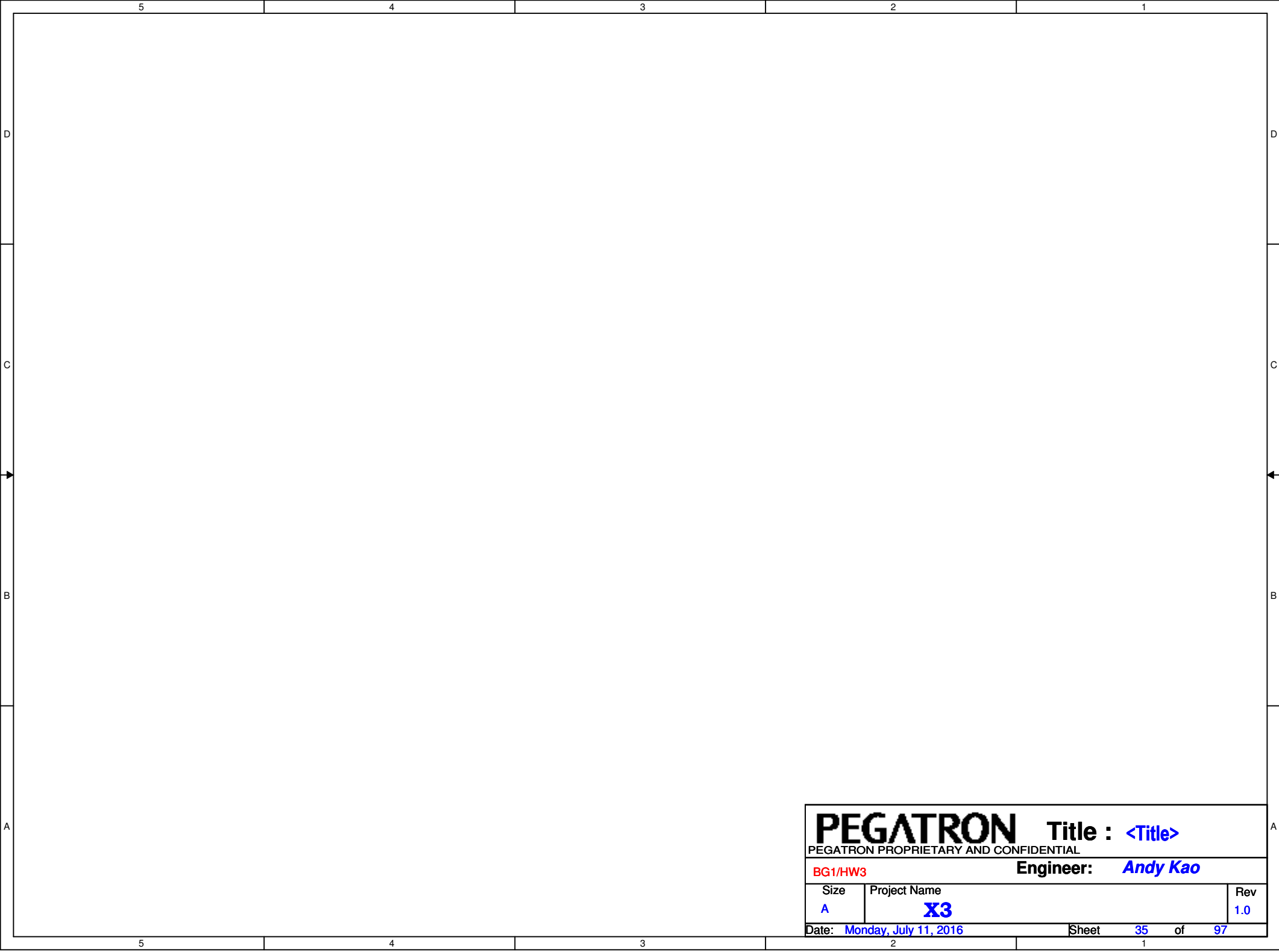
PEGATRON		Title : RST_Reset Circuit	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: Andy Kao	
Size B	Project Name X3		Rev 1.0
Date: Monday, July 11, 2016		Sheet 32 of 97	



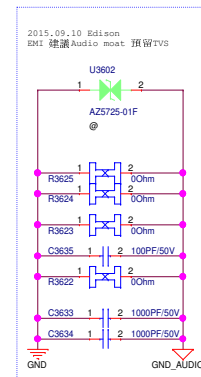
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PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: <i>Andy Kao</i>
Size A	Project Name X3	Rev 1.0
Date: Monday, July 11, 2016		Sheet 33 of 97



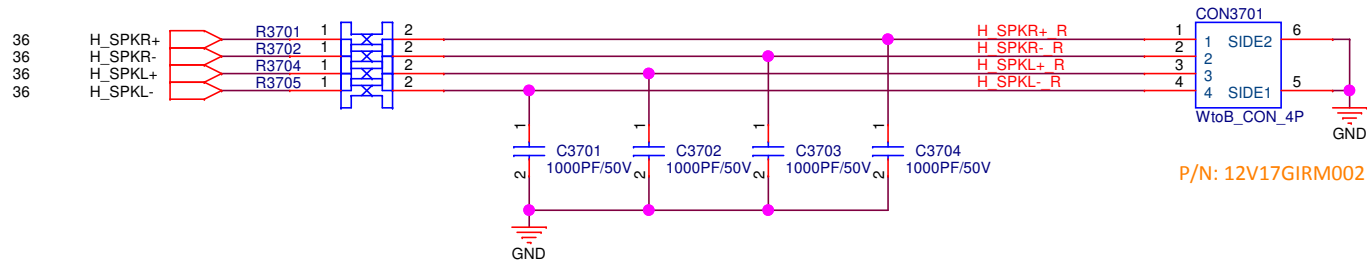
PEGATRON Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: Andy Kao
Size A	Project Name X3	Rev 1.0
Date: Monday, July 11, 2016		Sheet 34 of 97



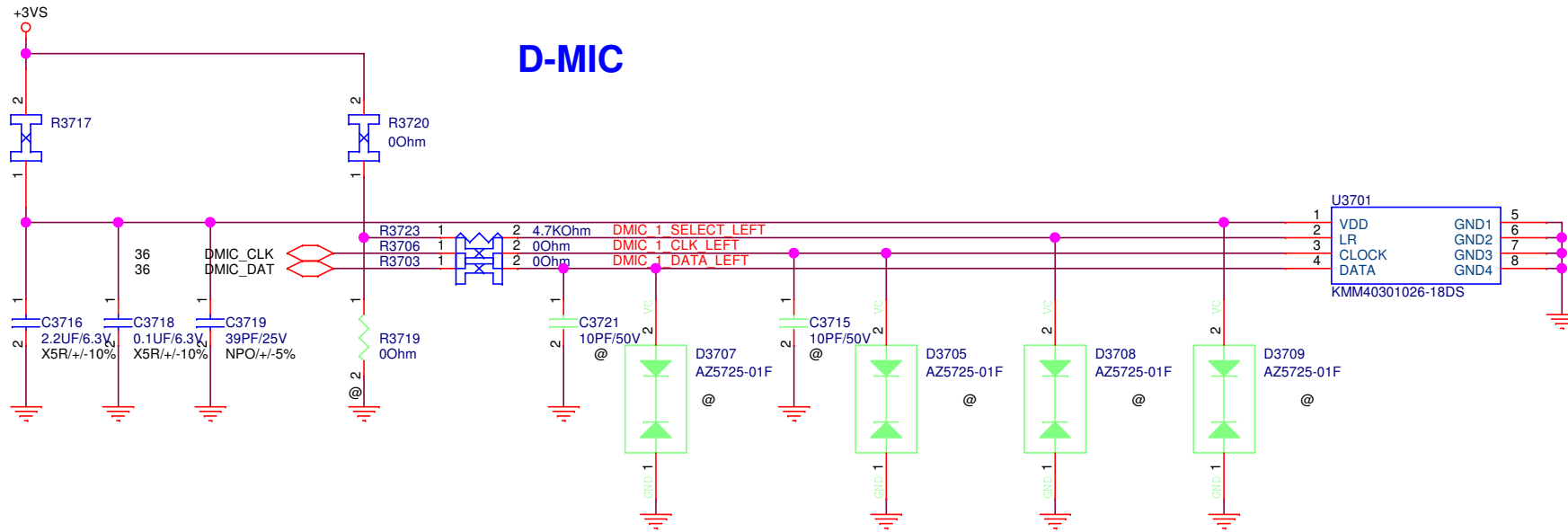
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size <i>A</i>	Project Name <i>X3</i>		Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>35</i> of <i>97</i>	

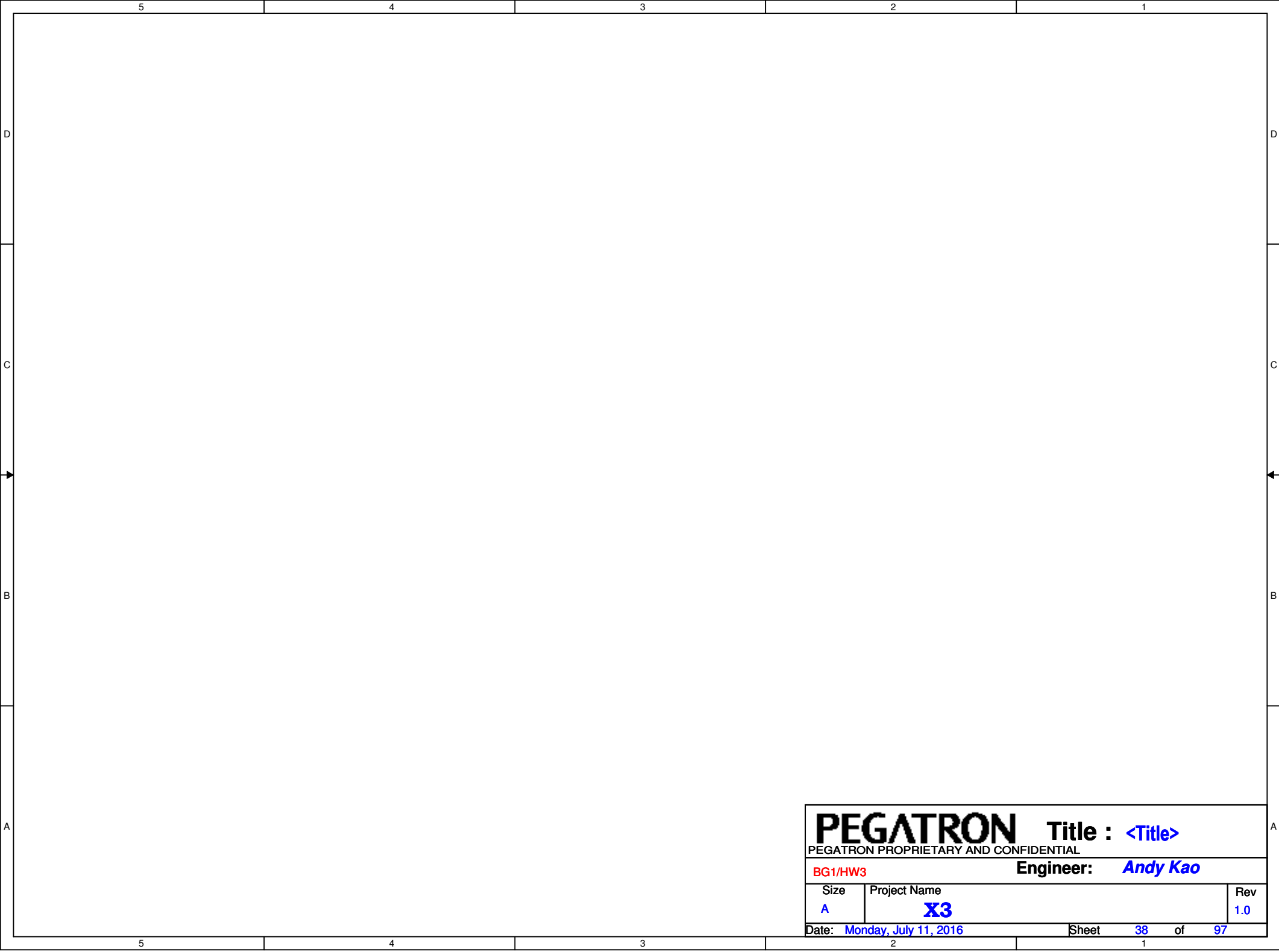


Speaker

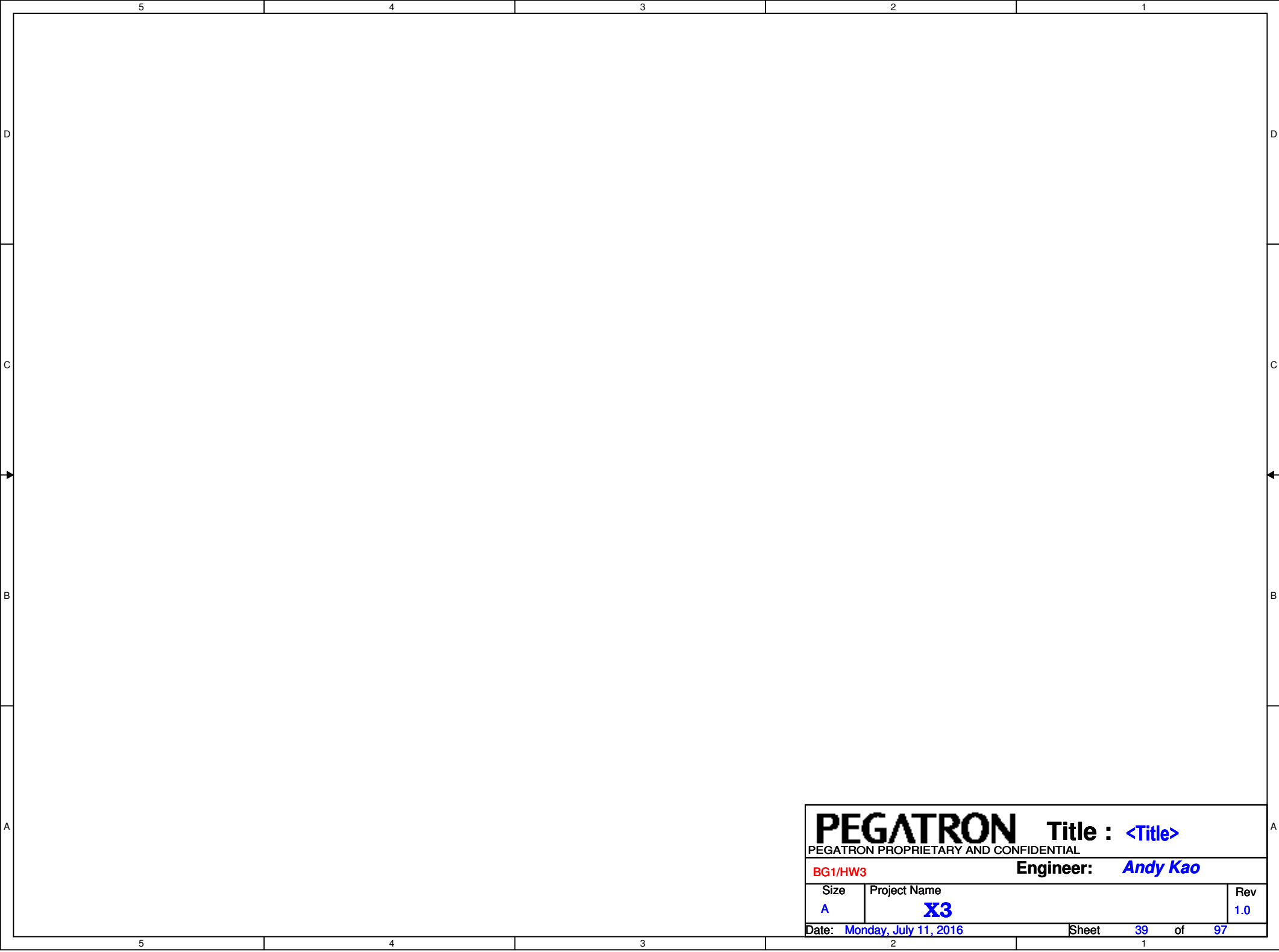


D-MIC

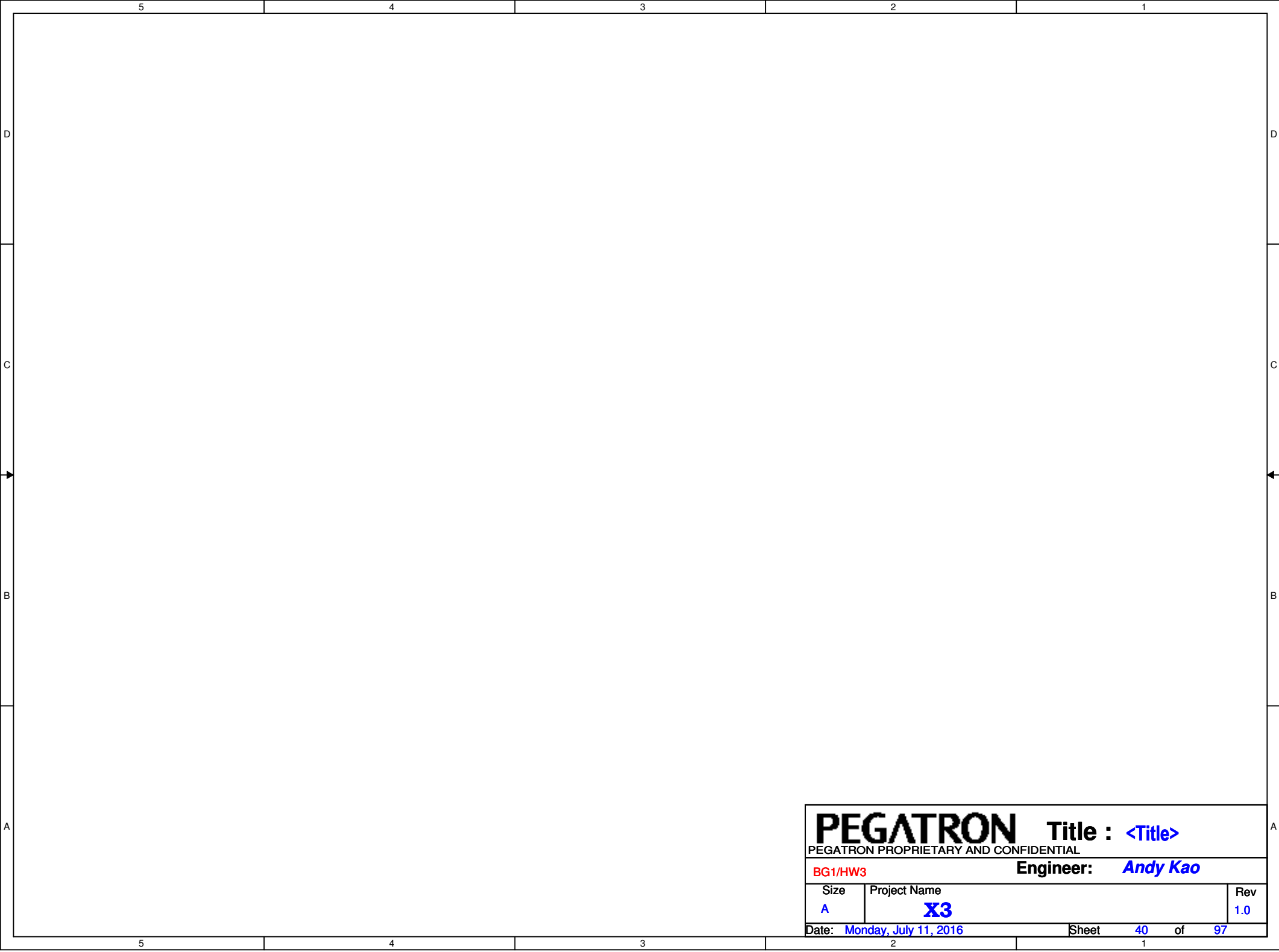




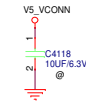
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size <i>A</i>	Project Name X3		Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>38</i> of <i>97</i>	



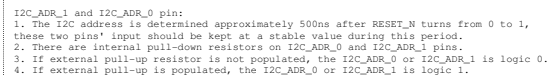
PEGATRON		Title : <Title>
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: <i>Andy Kao</i>
Size <i>A</i>	Project Name X3	Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>39</i> of <i>97</i>



PEGATRON		Title : <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size <i>A</i>	Project Name X3		Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>40</i> of <i>97</i>	



The DVDD_IO can be power supplied by 1.8V ~ 3.3V:
If AP's IO type is 1.8V, select 1.8V power for DVDD_IO;
If AP's IO type is 3.3V, select 3.3V power for DVDD_IO.



Engineer: Andy Kao		
Size C	Project Name X3	Rev 1.0
Date: Monday, July 11, 2016	Sheet 41 of 97	

Hardware Solution For Dead Battery

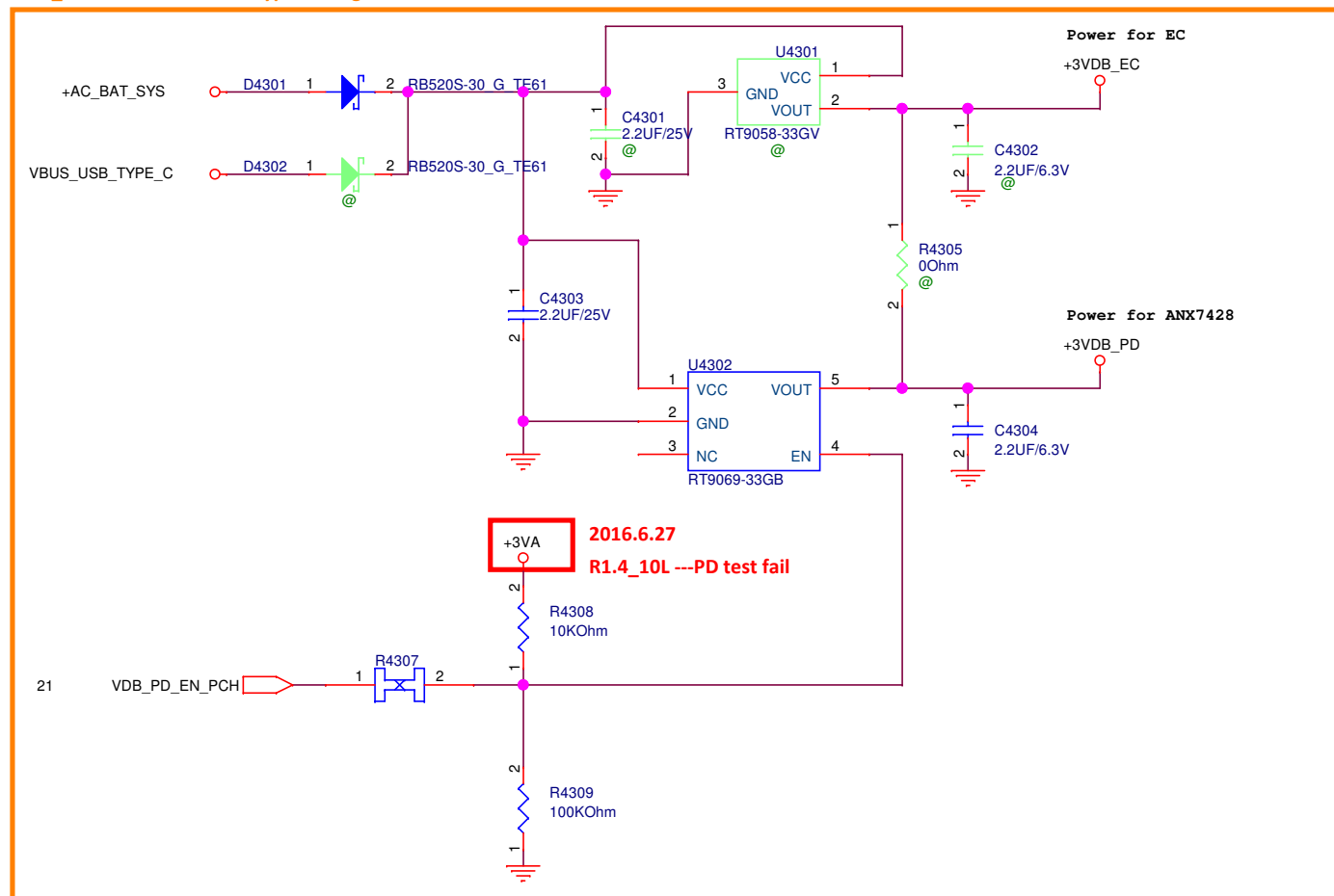
For notebook applications, if the battery charger needs higher voltage than 5V to operate correctly, execute the steps below in the order they are listed:

VBUS_USB_TYPE_C		VBUS_USB_TYPE_C	41,42
+AC_BAT_SYS		+AC_BAT_SYS	45,80,81,82,83,88
+3VDB_EC		+3VDB_EC	30
+3VDB_PD		+3VDB_PD	41

Requirement of U1:

- 1) Vin range: 4V-30V.
- 2) Vout: EC's operating voltage + Vf of D1
- 3) Output current >= EC's operating current.

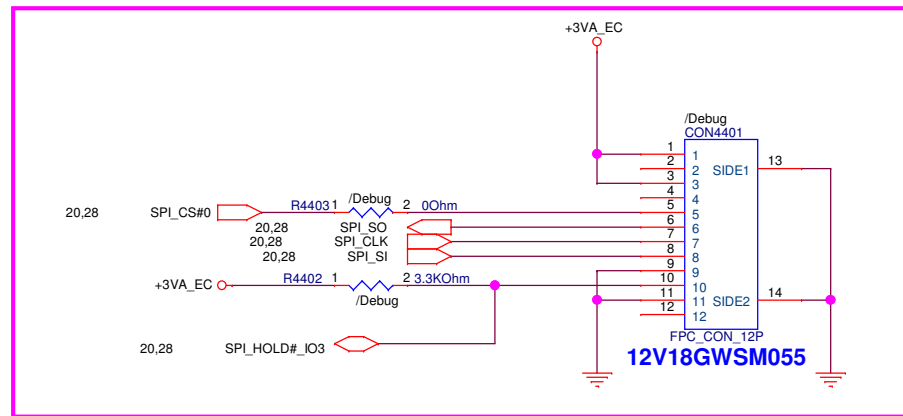
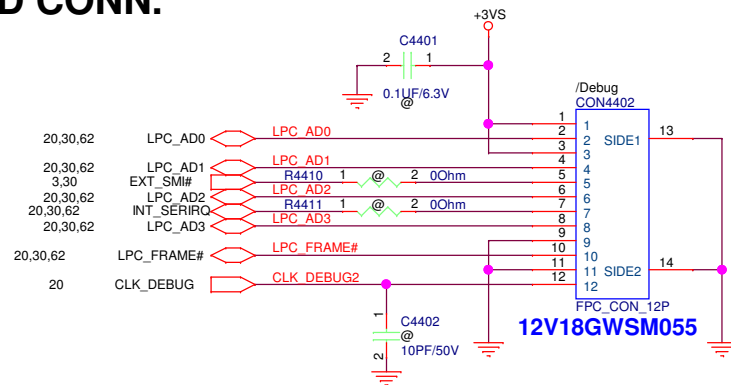
R1.0_10L ---Follow HAWAll type-c design



<Variant Name>

PEGATRON		Title : Dead Battery	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
Engineer: Andy Kao			
Size Custom	Project Name X3	Rev 1.0	
Date: Monday, July 11, 2016	Sheet 43 of 97		

DEBUG CARD CONN.

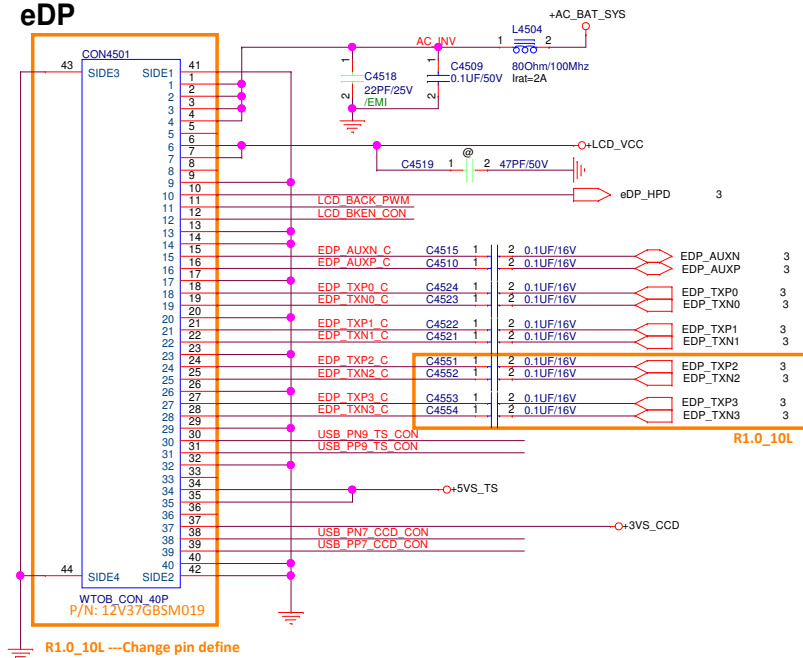


R1.1_10L ---BIOS request

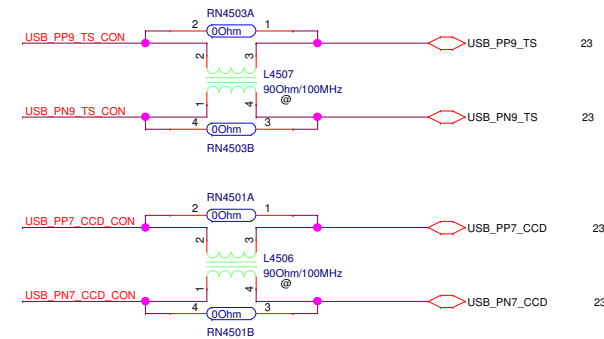
<Variant Name>

PEGATRON		Title : DEBUG CONN.	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: Andy Kao	
Size B	Project Name X3		Rev 1.0
Date: Monday, July 11, 2016		Sheet 44	of 97

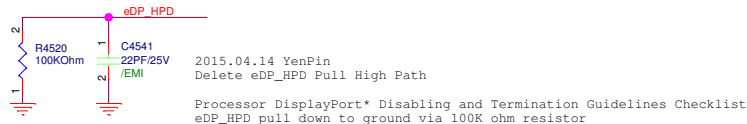
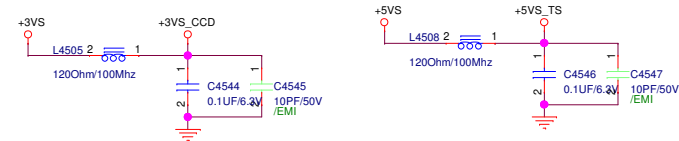
eDP



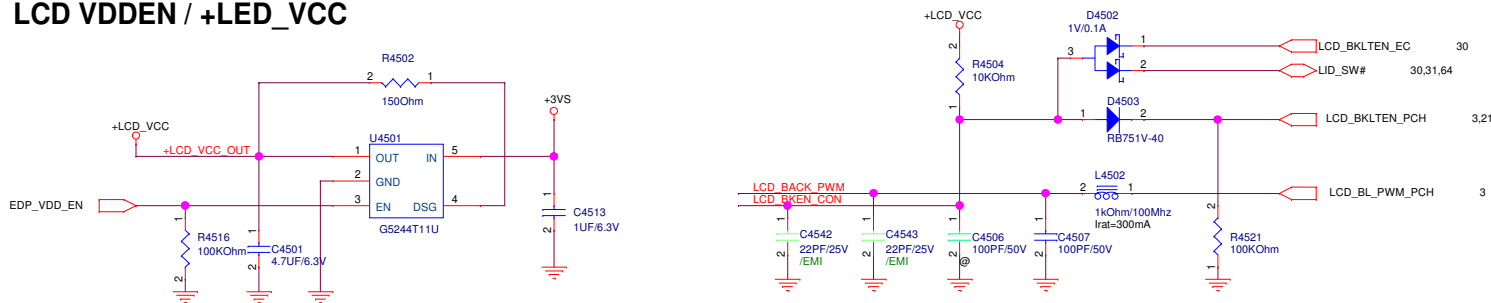
+3VS	+3VS	3,4,21,22,23,24,30,31,32,36,37,44,47,50,51,53,57,62,64,91,92
+5VS	+5VS	31,36,48,50,51,57,80,91
+AC_BAT_SYS	+AC_BAT_SYS	43,80,81,82,83,88



Camera



LCD VDDEN / +LED_VCC



<Variant Name>

PEGATRON		Title : eDP CONN	
Size	Project Name	Engineer:	Andy Kao
Custom	X3		
Date:	Monday, July 11, 2016	Sheet	45 of 97
Rev	1.0		

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T4702 1 PRE

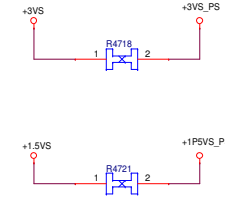
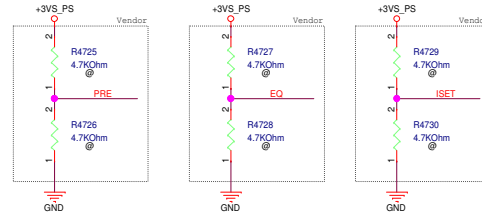
Output pre-emphasis setting; Internal pull down at -150kΩ, 3.3V I/O.
L: no pre-emphasis
H: 1.6dB pre-emphasis
M: 2.5dB pre-emphasis

T4701 1 EQ

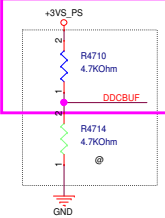
Receiver equalization setting; Internal pull down at -150kΩ, 3.3V I/O.
L: programmable EQ for channel loss up to 12.6dB
H: programmable EQ for channel loss up to 4.3dB
M: programmable EQ for channel loss up to 8.6dB

T4703 1 ISET

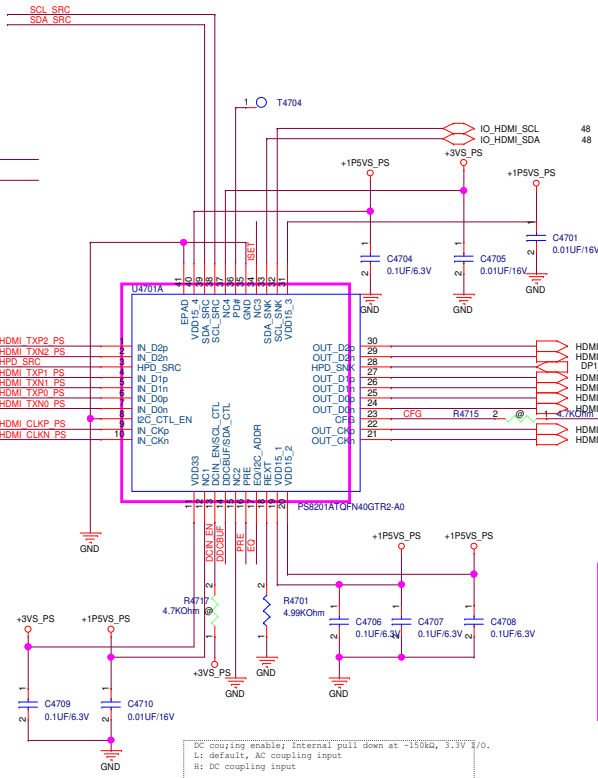
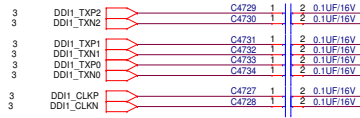
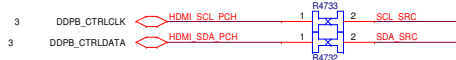
TMDS output swing adjustment; Internal pull down at -150kΩ, 3.3V I/O.
L: default
H: increase +13%
M: reduce -13%



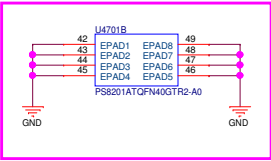
R1.1_10L ---Follow megatron



Enable active DDC buffer; Internal pull down at -150kΩ, 3.3V I/O.
L: default, passive DDC pass-through
H: active DDC buffer with default threshold
M: active DDC buffer without internal pull up resistor



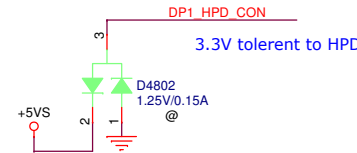
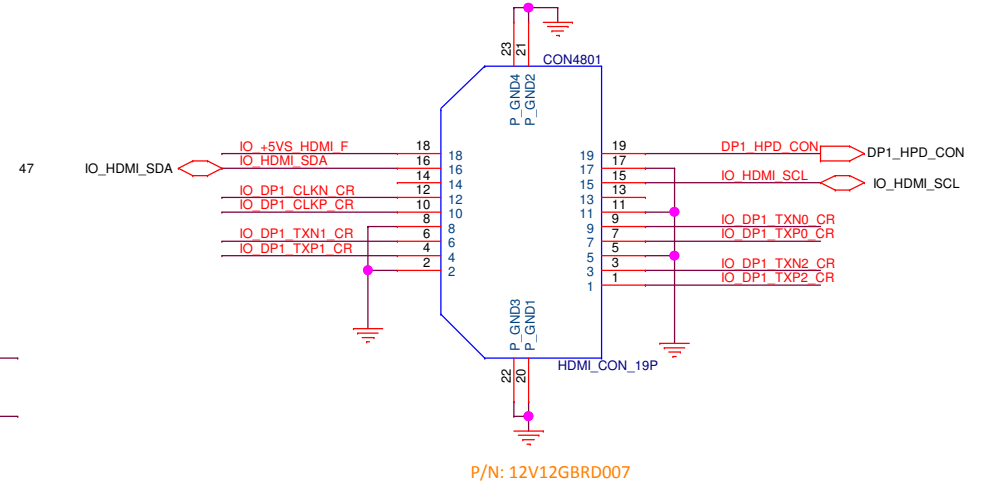
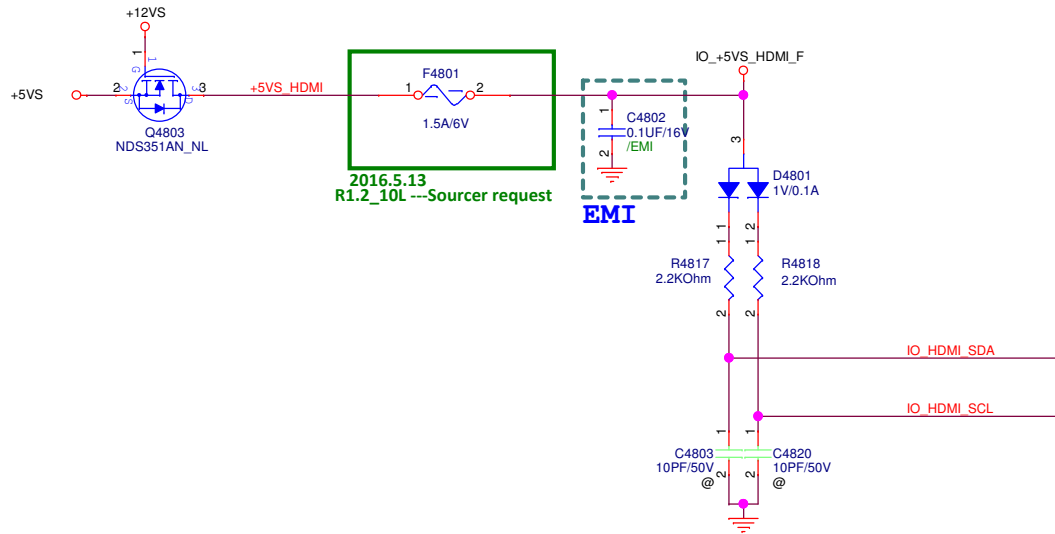
Configuration pin, 3.3V I/O, internal pull down at -150kΩ, 3.3V I/O.
L: HDMI ID disable
H: HDMI ID enable
(Typ:1.5V; Max:1.53V; Min:1.47V)



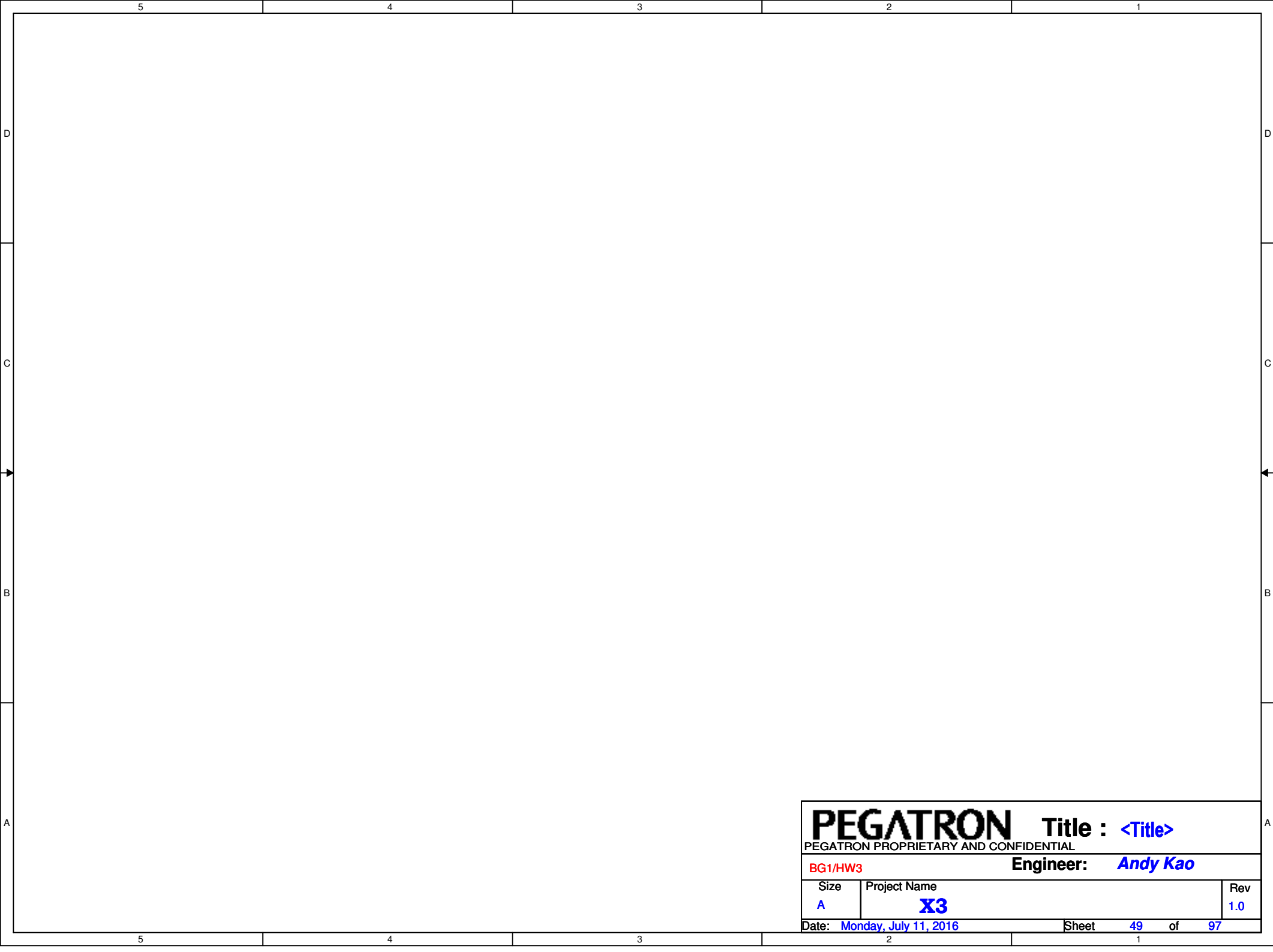
DC coupling enable; Internal pull down at -150kΩ, 3.3V I/O.
L: default, AC coupling input
H: DC coupling input

HDMI

+3VS	+3VS	3,4,21,22,23,24,30,31,32,36,37,44,45,47,50,51,53,57,62,64,91,92
+5VS	+5VS	31,36,45,50,51,57,80,91
+12VS	+12VS	31,57,91



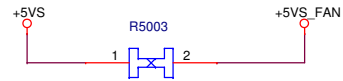
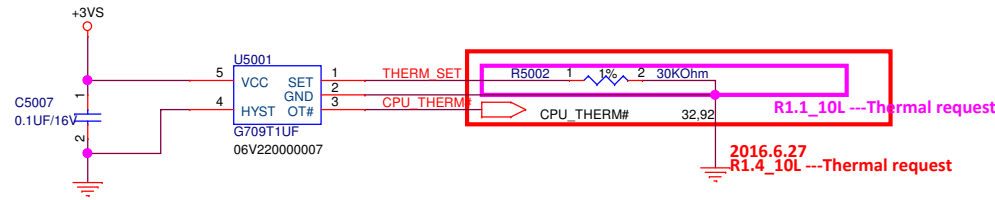
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: Andy Kao	
Size B	Project Name X3		Rev 1.0
Date: Monday, July 11, 2016	Sheet 48	of 97	



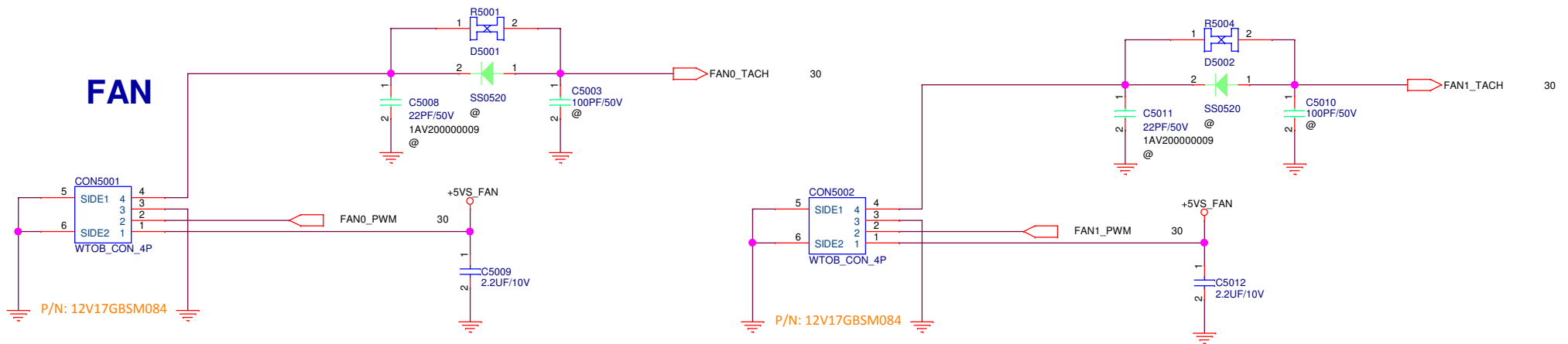
Thermal Sensor

temp setting : 80 degree

$RSET(k\Omega) = 0.0012T^{\circ}C - 0.9308T + 96.147$



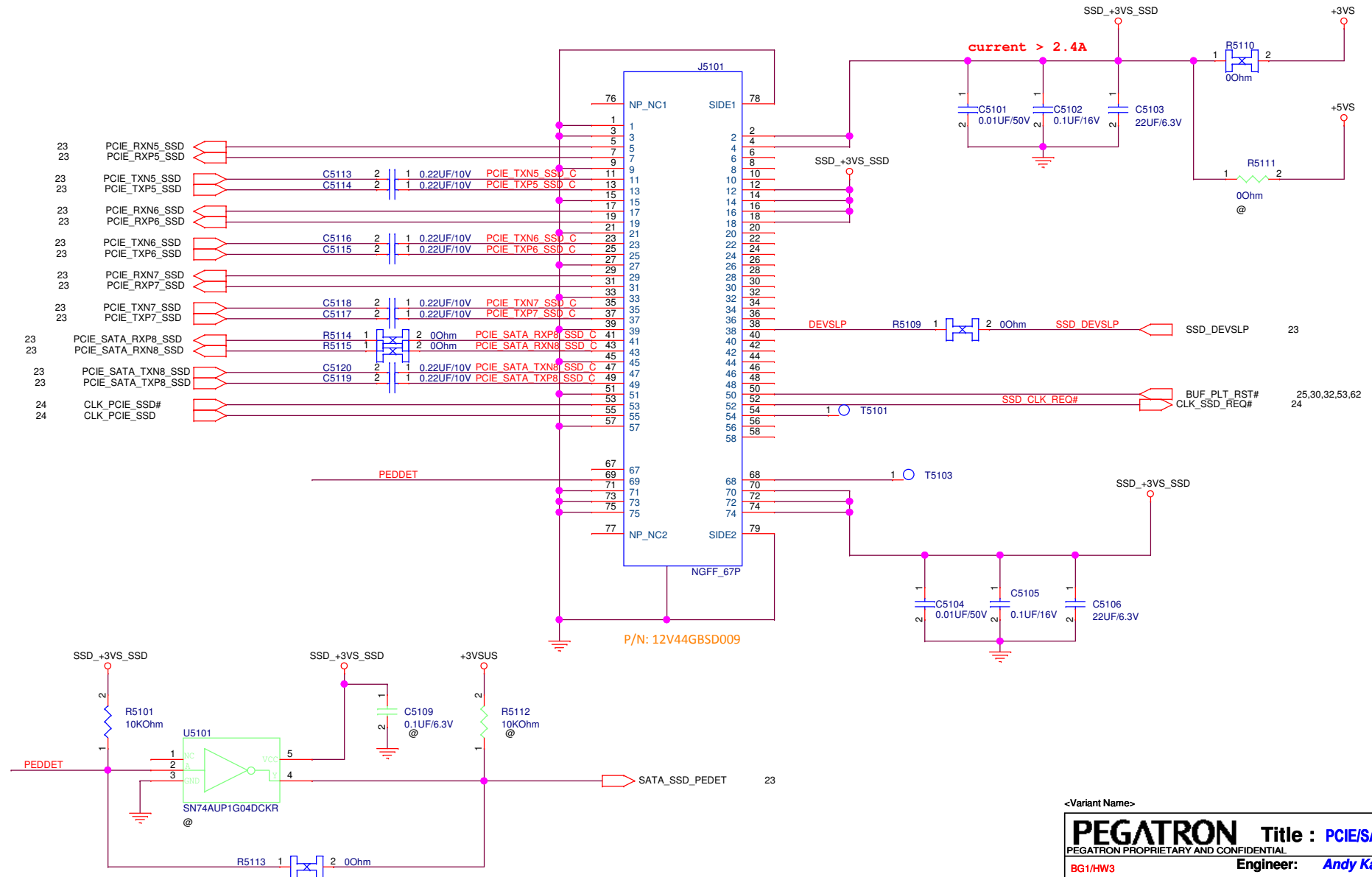
FAN



<Variant Name>

PEGATRON		Title : Thermal/Fan	
BG1/HW3		Engineer: Andy Kao	
Size	Project Name	Rev	
B	X3	1.0	
Date: Monday, July 11, 2016		Sheet	50 of 97

SSD(SATA/PCIE x4) NGFF socket (M-key)

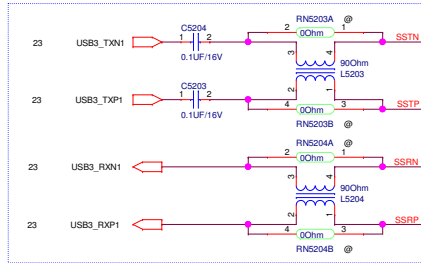


<Variant Name>

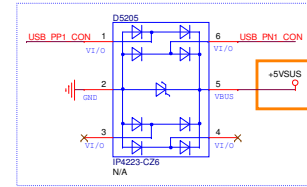
PEGATRON		Title : PCIE/SATA SSD	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: Andy Kao	
Size	Project Name		Rev
Custom	X3		1.0
Date: Monday, July 11, 2016		Sheet 51 of 97	

USB 3.0

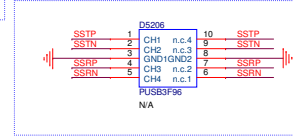
USB3.0 Choke



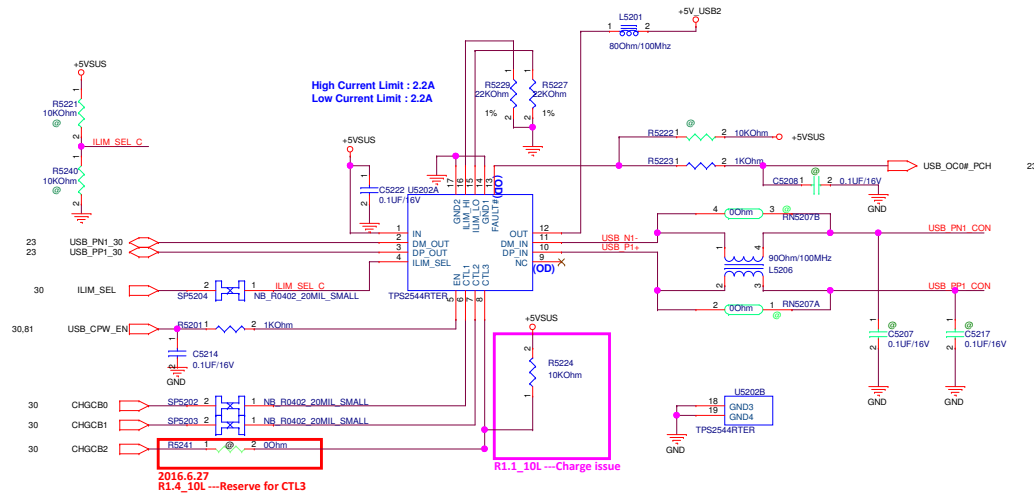
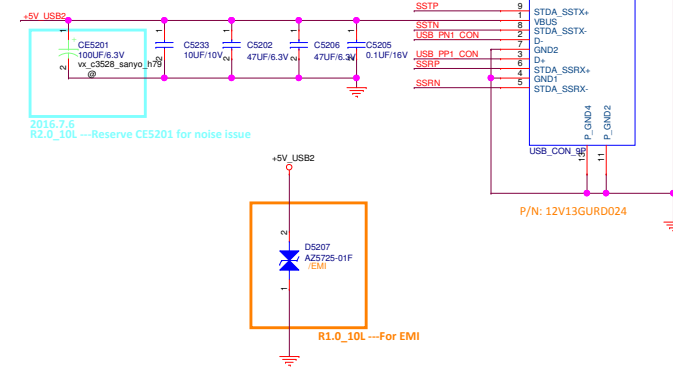
USB2.0 ESD



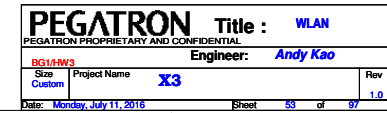
USB3.0 ESD

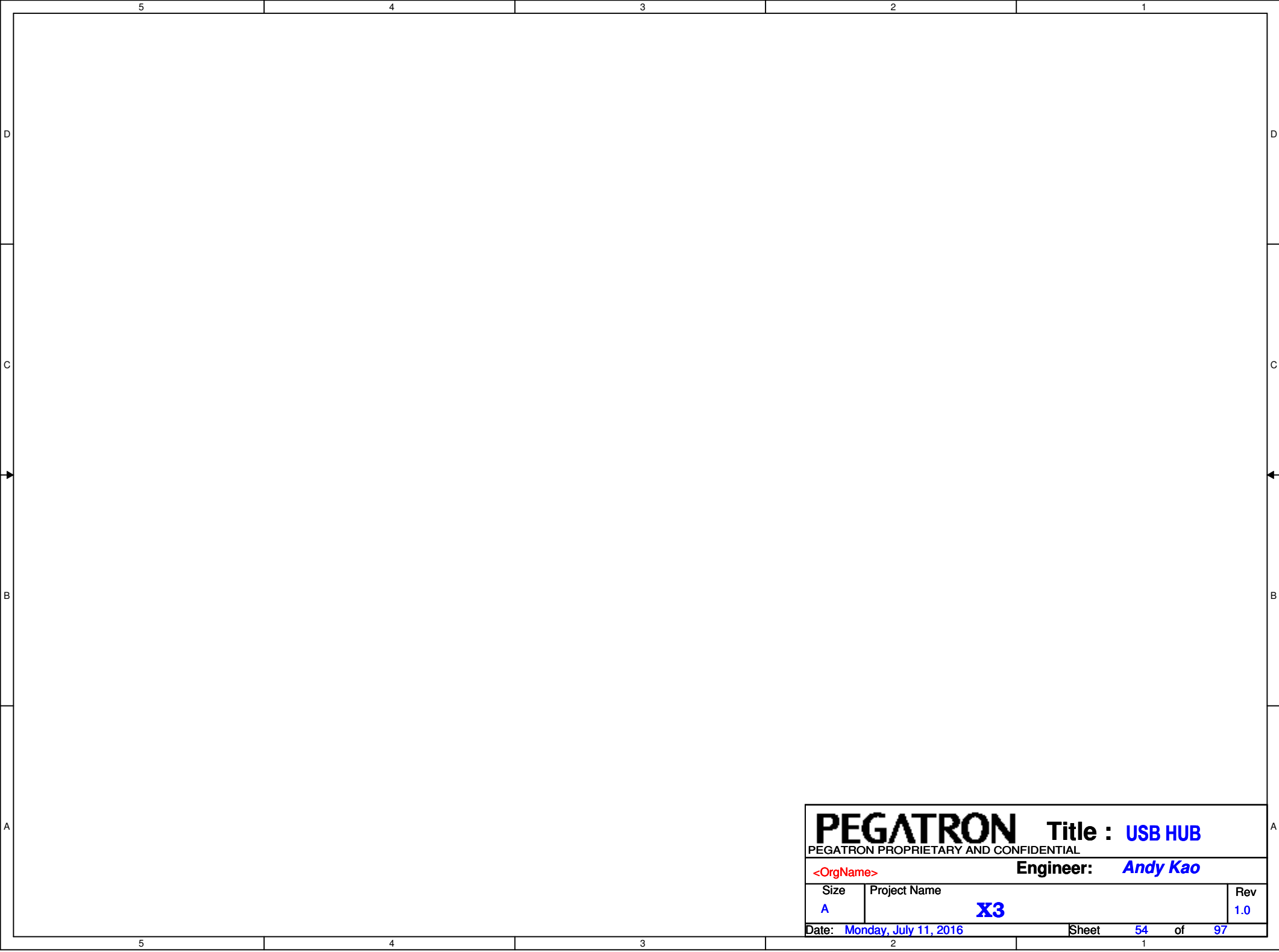


USB 3.0 - Type A



+3VS +3VS 3,4,21,22,23,24,30,31,32,36,37,44,45,47,50,51,57,62,64,91,92





PEGATRON

Title : USB HUB

PEGATRON PROPRIETARY AND CONFIDENTIAL

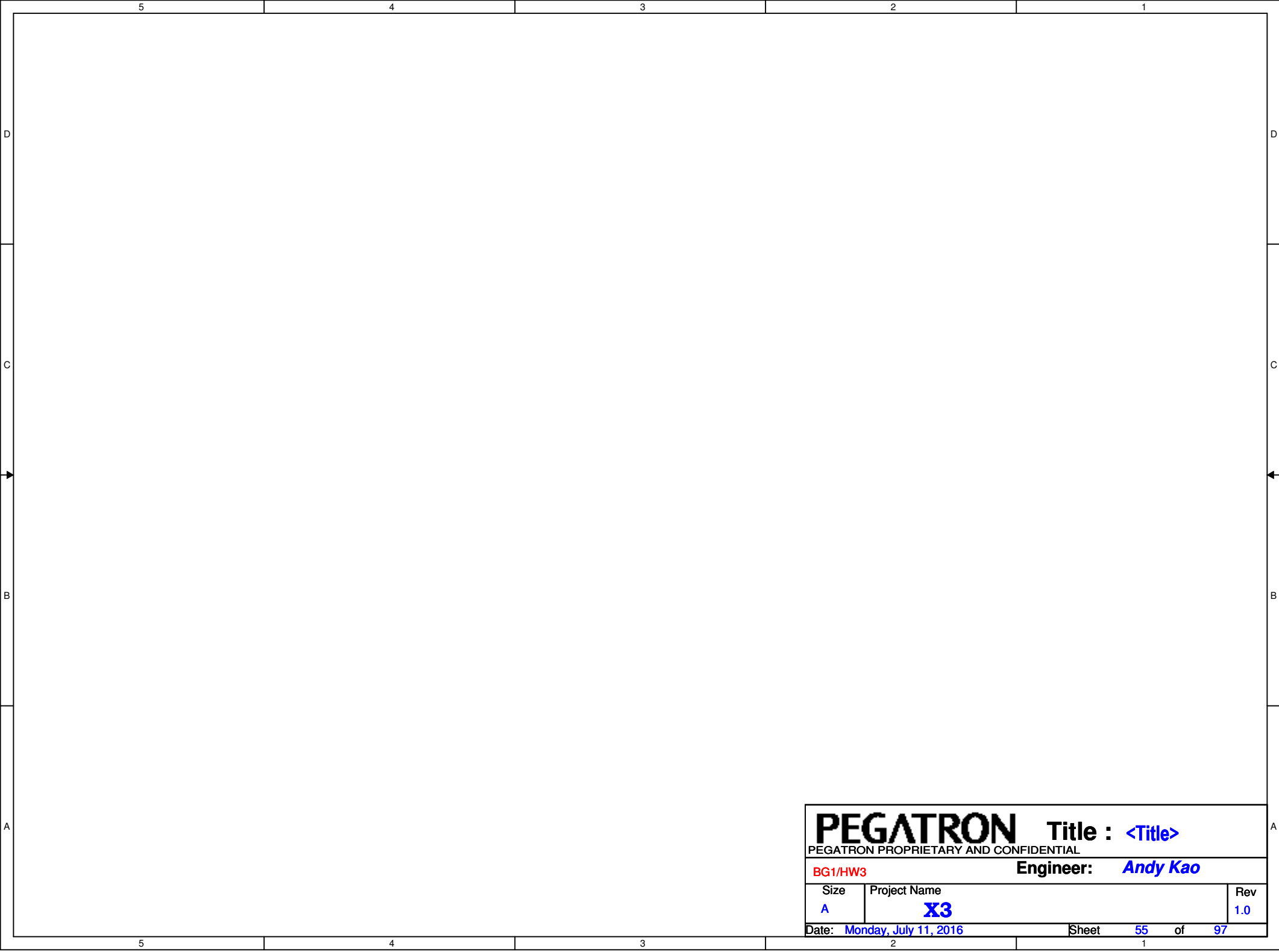
<OrgName>

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016

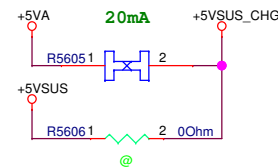
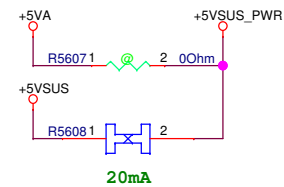
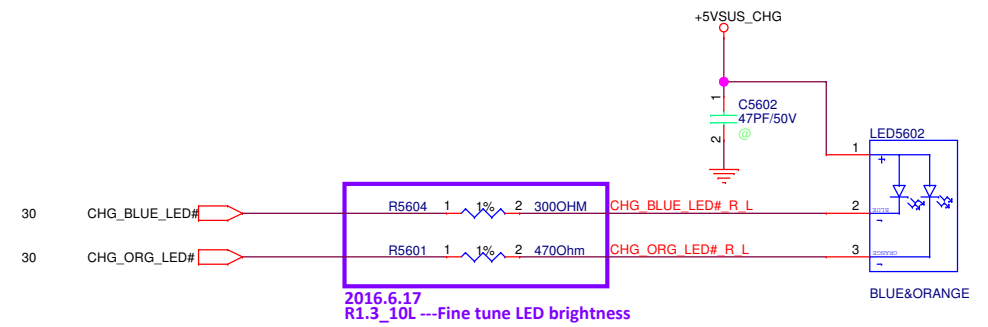
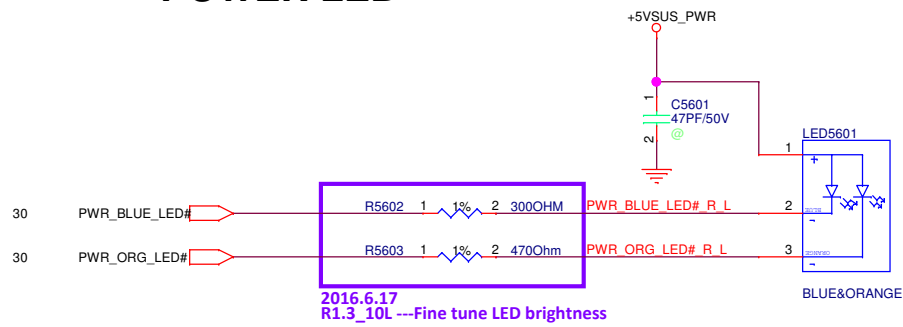
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PEGATRON		Title : <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size <i>A</i>	Project Name X3		Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>55</i> of <i>97</i>	

POWER LED

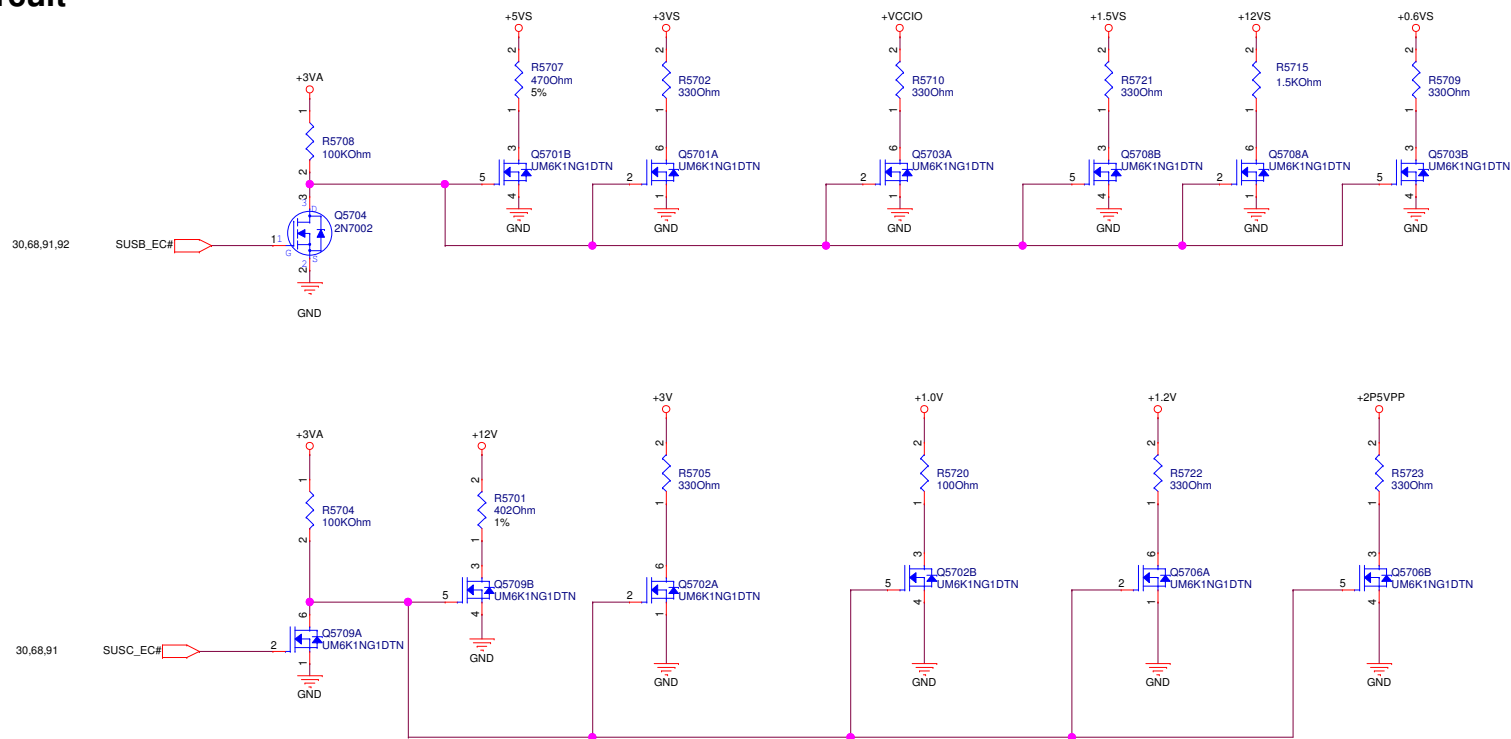
Charger LED



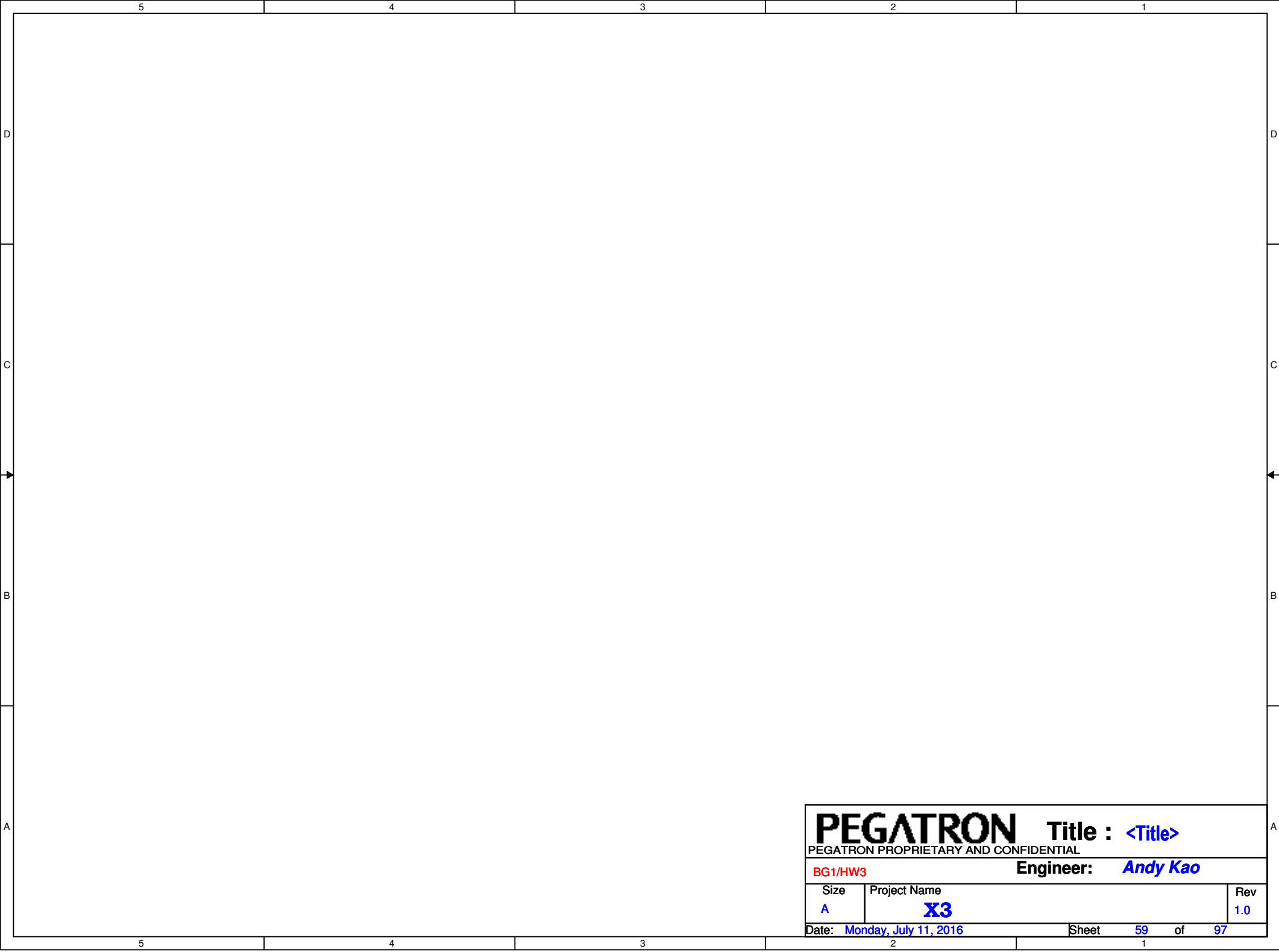
<Variant Name>

PEGATRON		Title : LED_Indicator	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: Andy Kao	
Size B	Project Name X3		Rev 1.0
Date: Monday, July 11, 2016		Sheet 56	of 97

Discharge Circuit

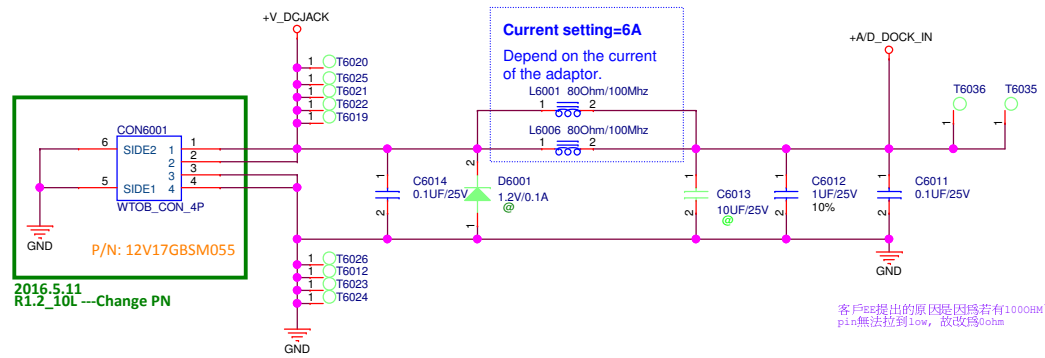


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PEGATRON										Title : <Title>																																																																																																								
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BG1/HW3										Engineer: Andy Kao																																																																																																								
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Date: Monday, July 11, 2016										Sheet 58 of 97																																																																																																								
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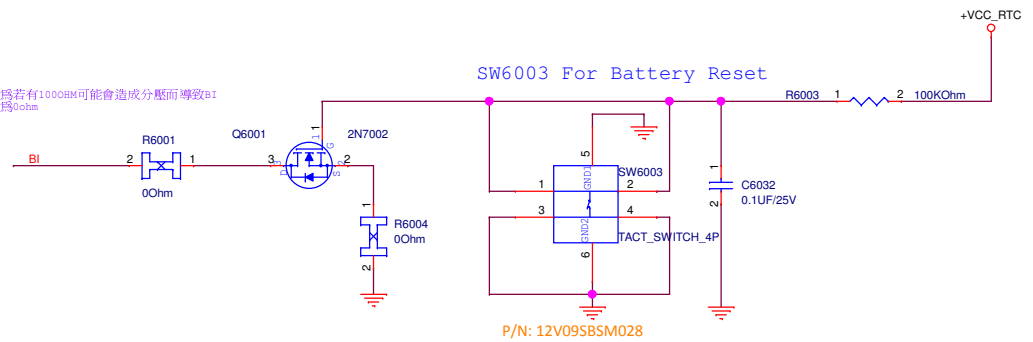
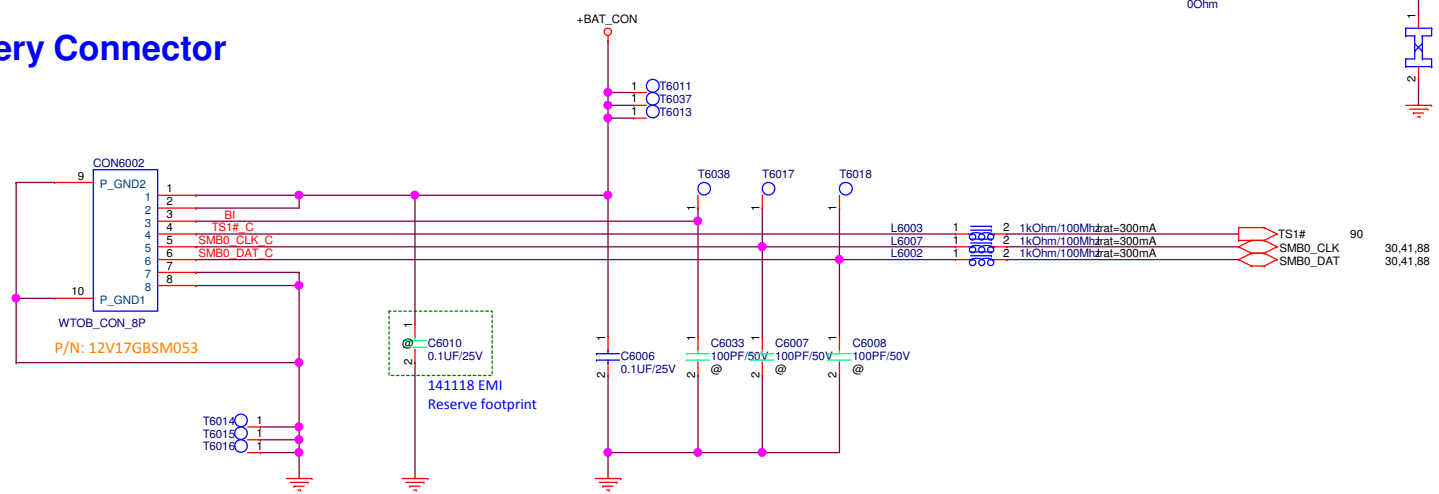


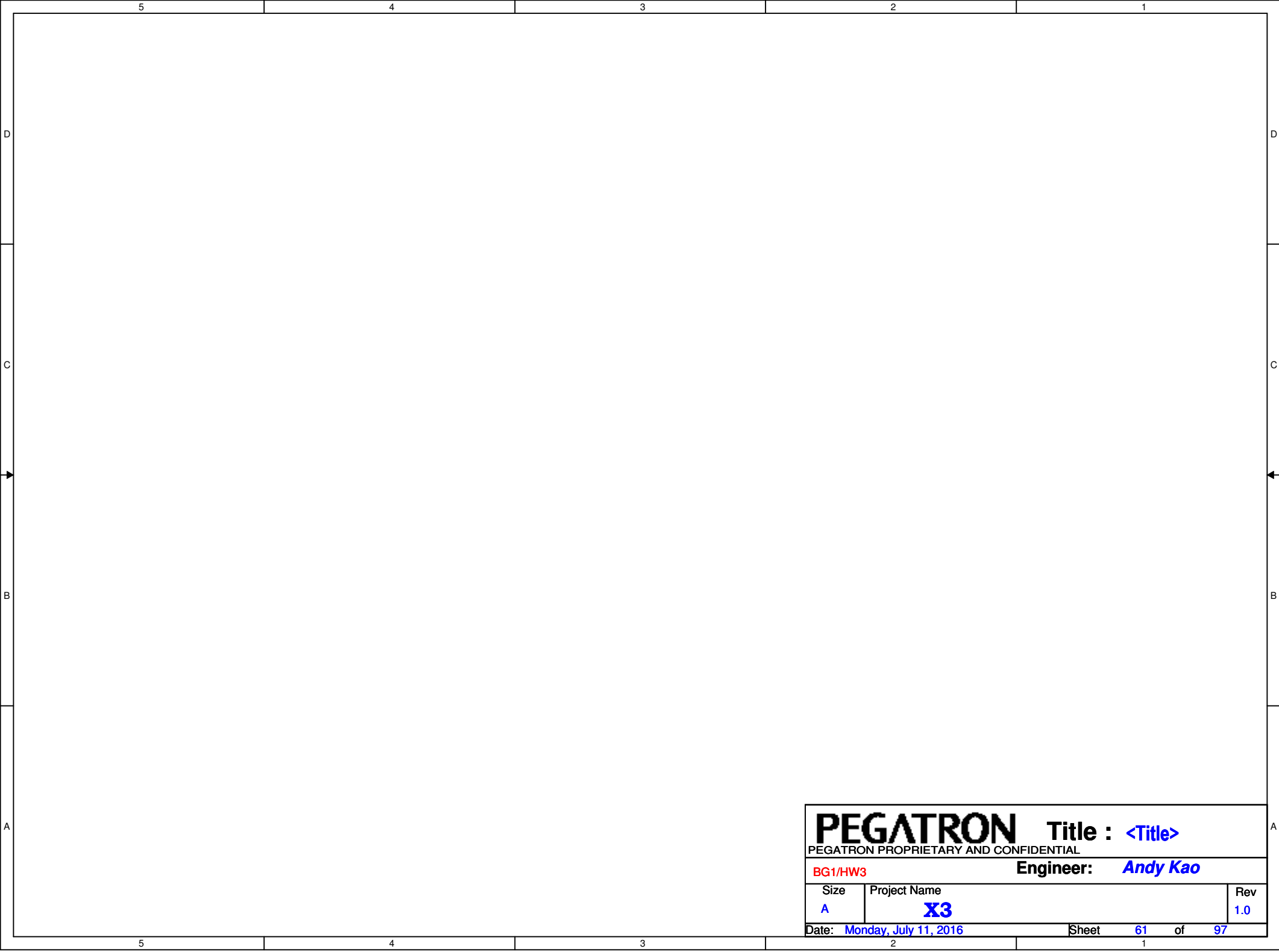
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size <i>A</i>	Project Name X3		Rev <i>1.0</i>
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DC Jack WtoB CONN

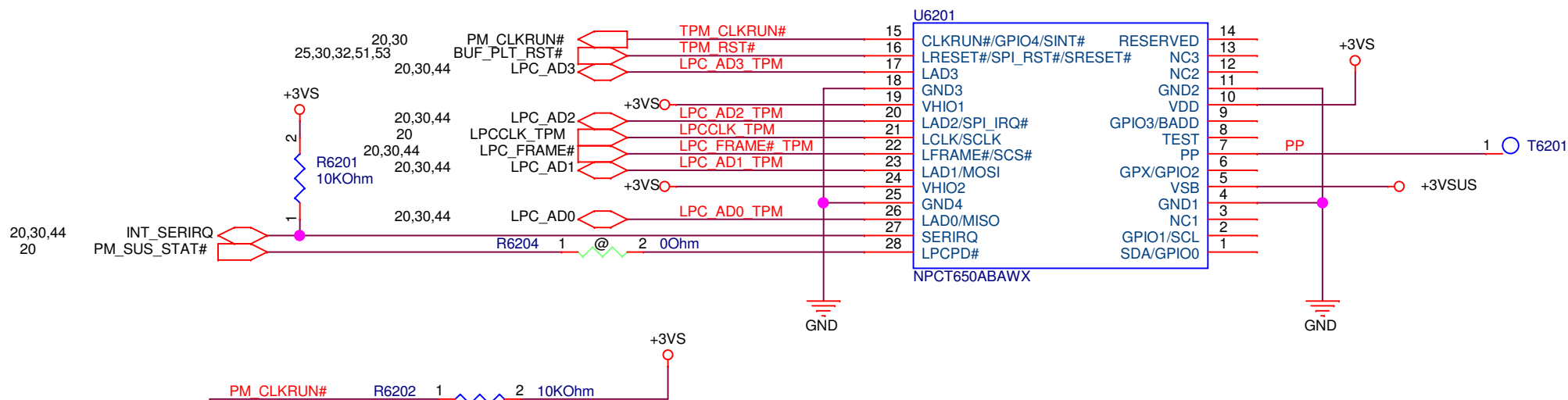
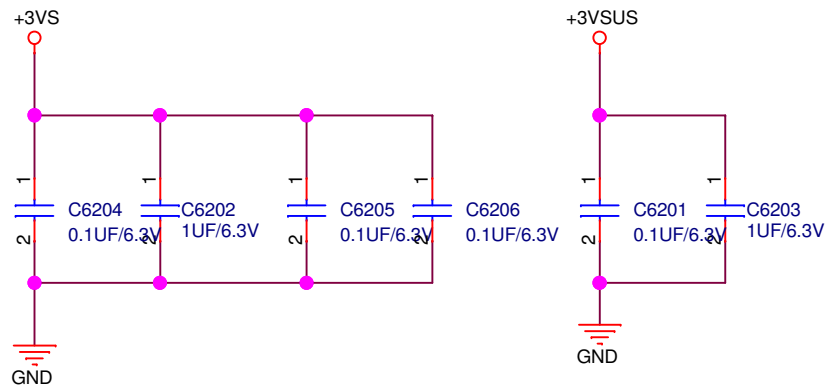


Battery Connector





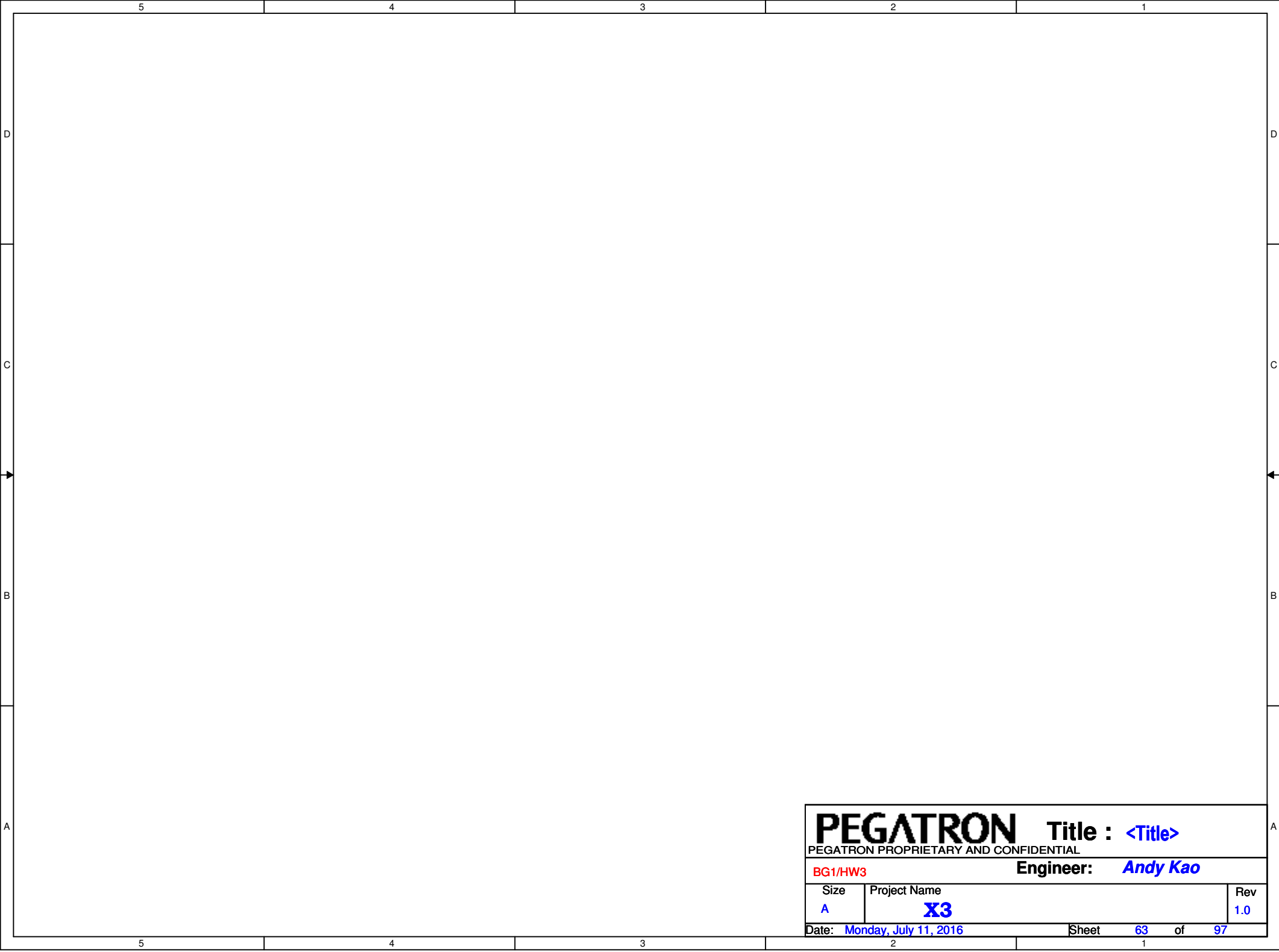
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PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: <i>Andy Kao</i>
Size A	Project Name X3	Rev 1.0
Date: Monday, July 11, 2016		Sheet 61 of 97



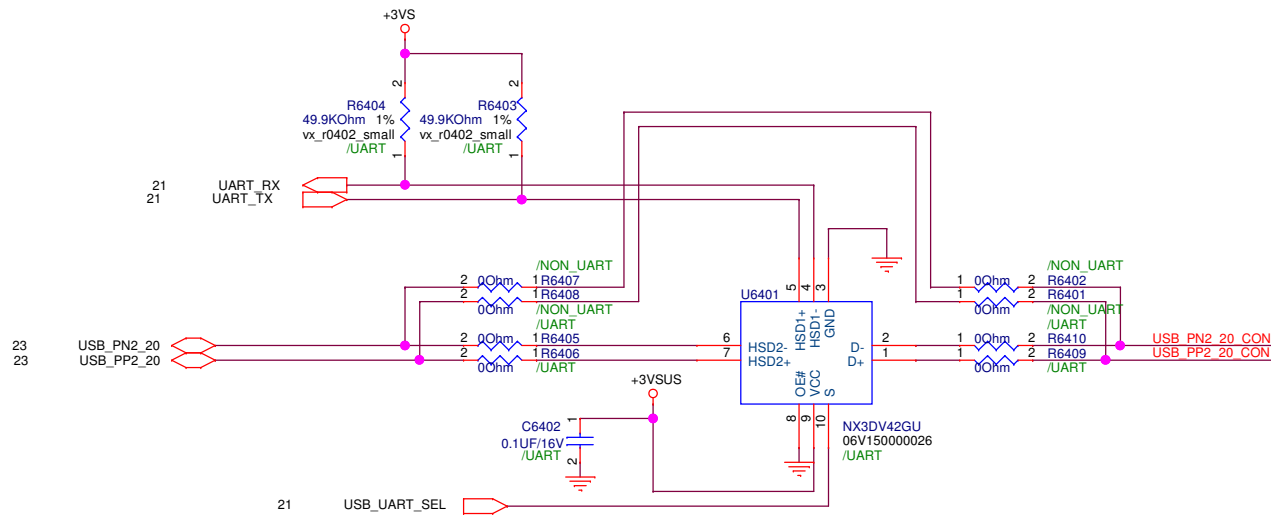
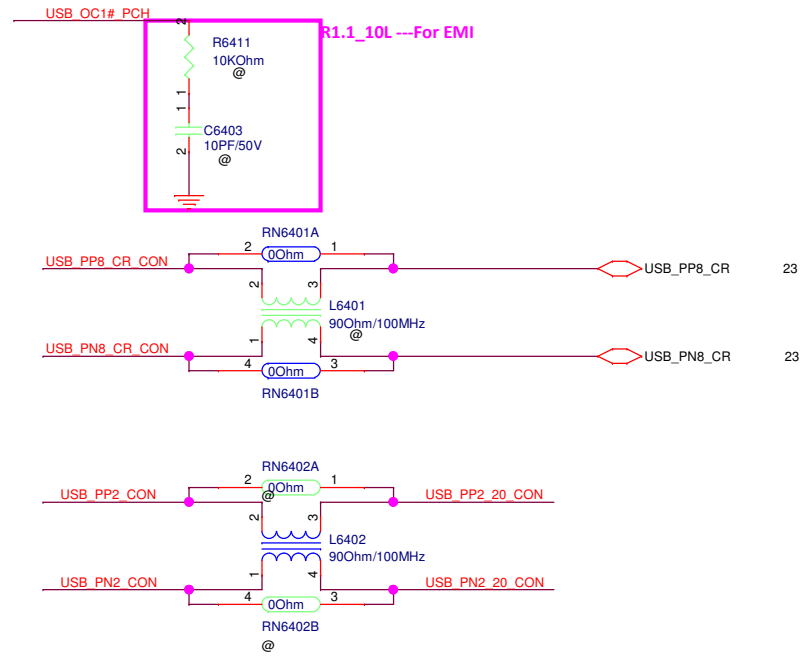
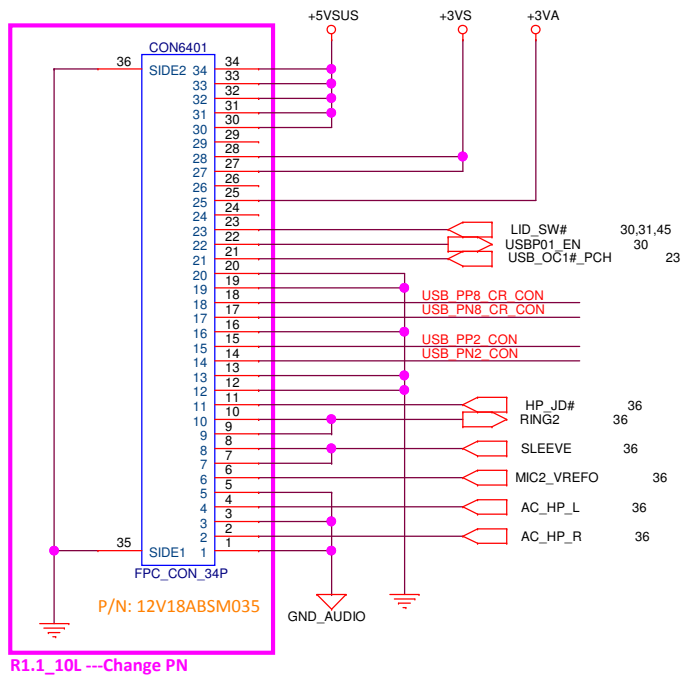
Vendor Suggest Pull High Resistor Need To Close To TPM
PM_CLKRUN#, INT_SERIRQ Need To Pull 10Kohm To+3VS at Chipset Side

<Variant Name>

PEGATRON		Title : TPM CONN	
BG1/HW3		Engineer: Andy Kao	
Size Custom	Project Name X3		Rev 1.0
Date: Monday, July 11, 2016		Sheet 62 of 97	



PEGATRON		Title : <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size <i>A</i>	Project Name X3		Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>63</i> of <i>97</i>	

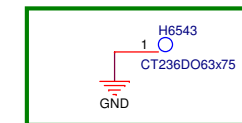
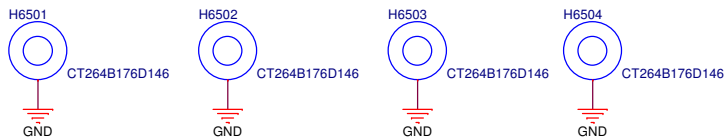


<Variant Name>		
PEGATRON Title : IO CON.		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3	Engineer: Andy Kao	
Size B	Project Name X3	Rev 1.0
Date: Monday, July 11, 2016	Sheet 64 of 97	

CPU NUT

6*2.5mm*1

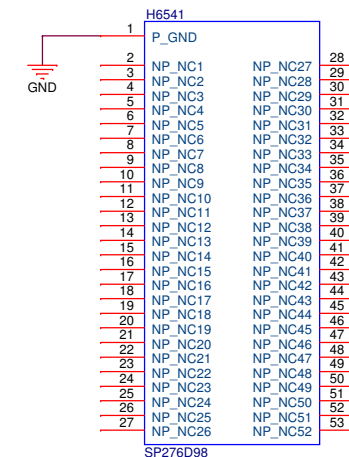
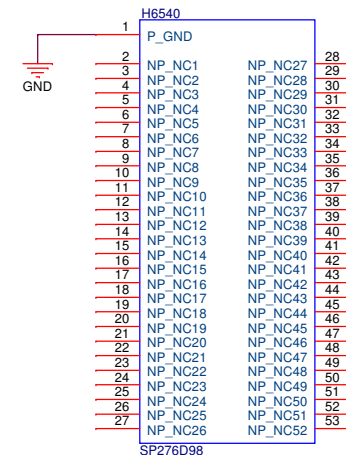
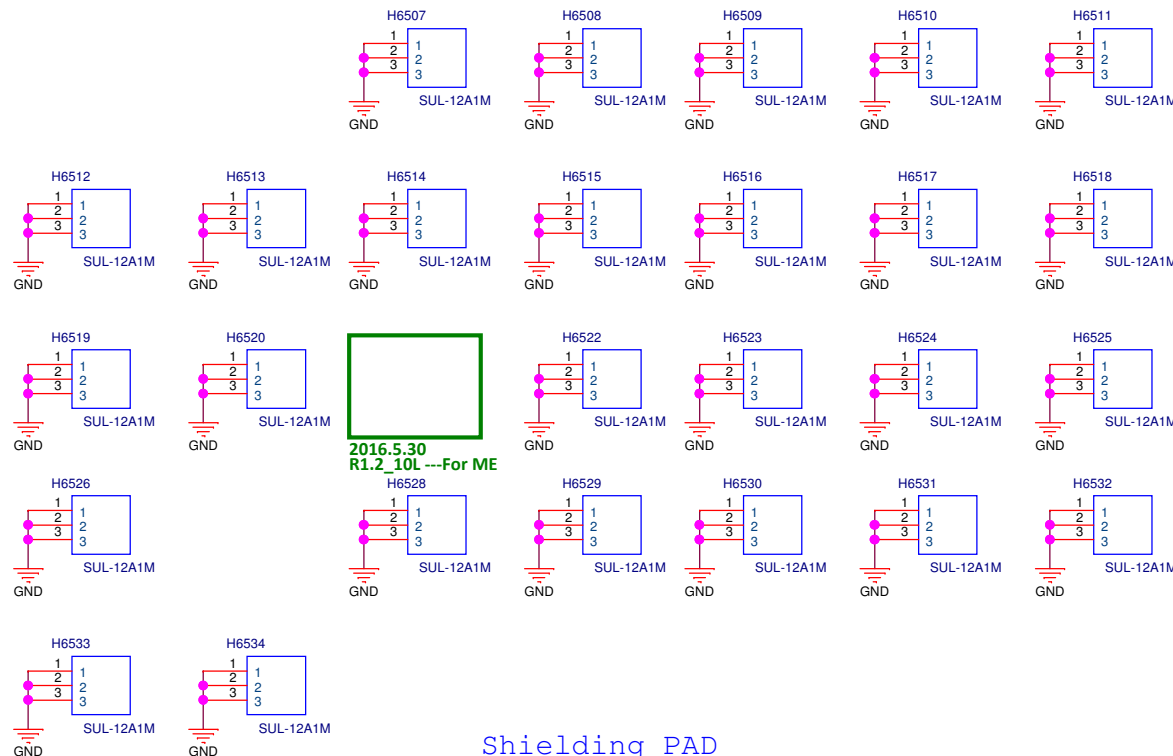
6*3.1mm*1



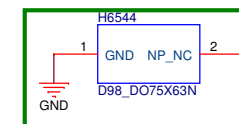
2016.6.6 R1.2_10L ---For ME

CLIP

Thermal screw*2

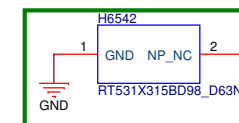


14*8mm*1



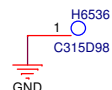
2016.6.6 R1.2_10L ---For ME

13.5*8mm*1

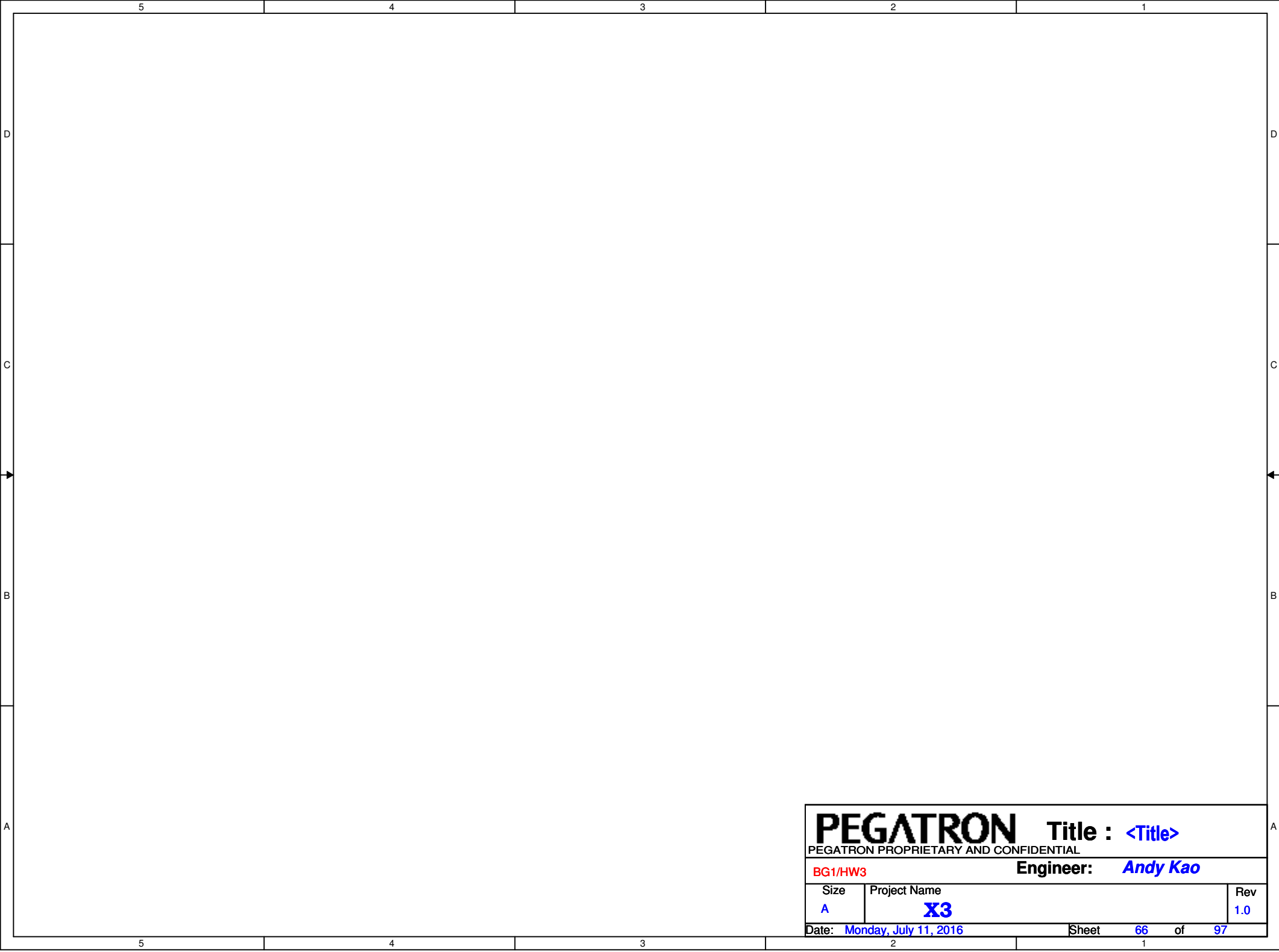


2016.6.6 R1.2_10L ---For ME

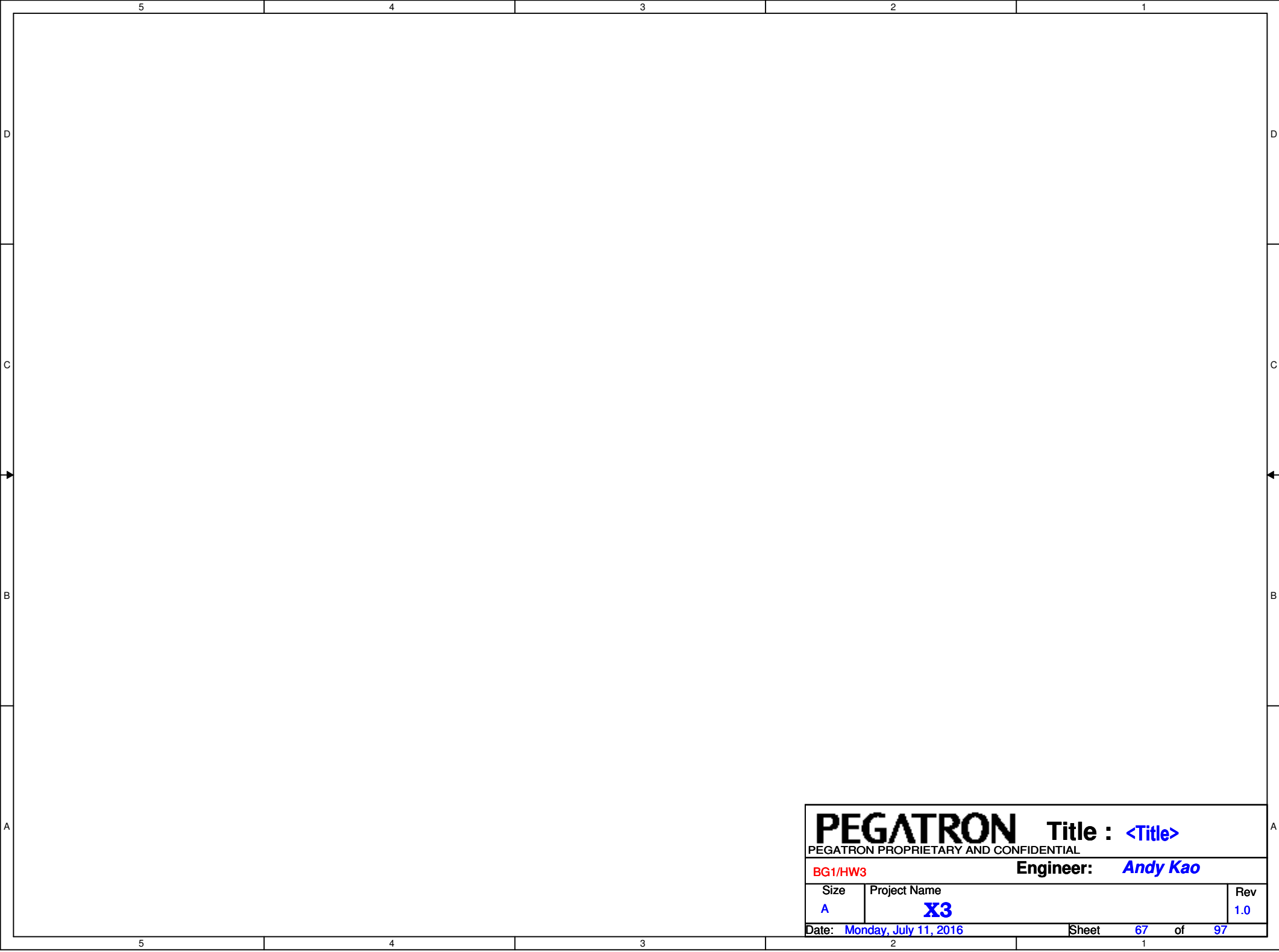
Shielding PAD



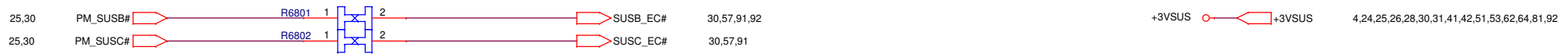
PEGATRON		Title : NUT,Screw Hole	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: Andy Kao	
Size B	Project Name X3		Rev 1.0
Date: Monday, July 11, 2016		Sheet 65 of 97	



PEGATRON		Title : <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size <i>A</i>	Project Name X3		Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>66</i> of <i>97</i>	

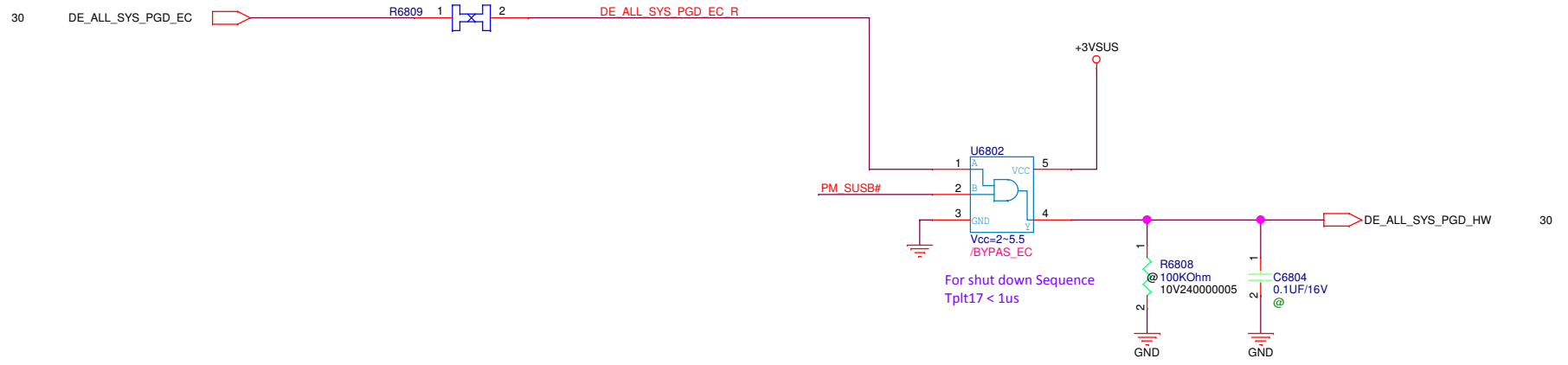


PEGATRON		Title : <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size <i>A</i>	Project Name X3		Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>67</i> of <i>97</i>	

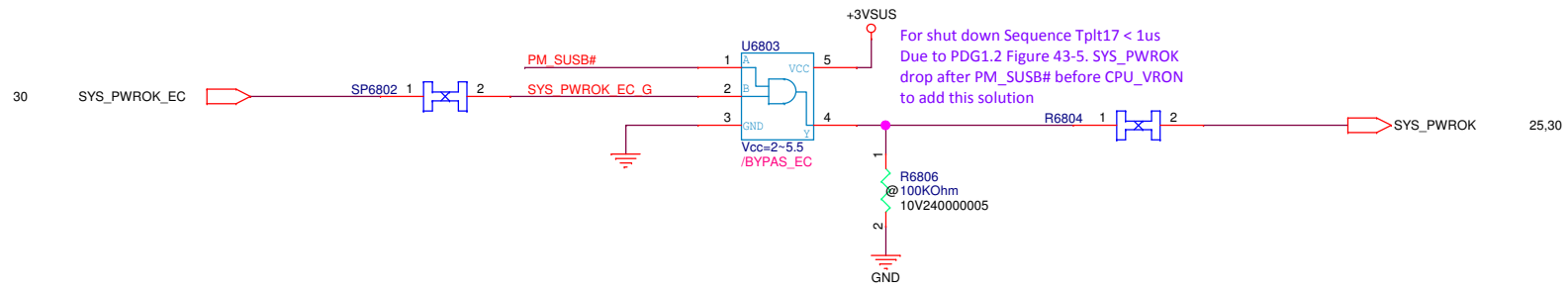


For Intel power sequence requestment
ALL_SYS_PWRGD to Delay_ALL_SYS_PGD >2ms

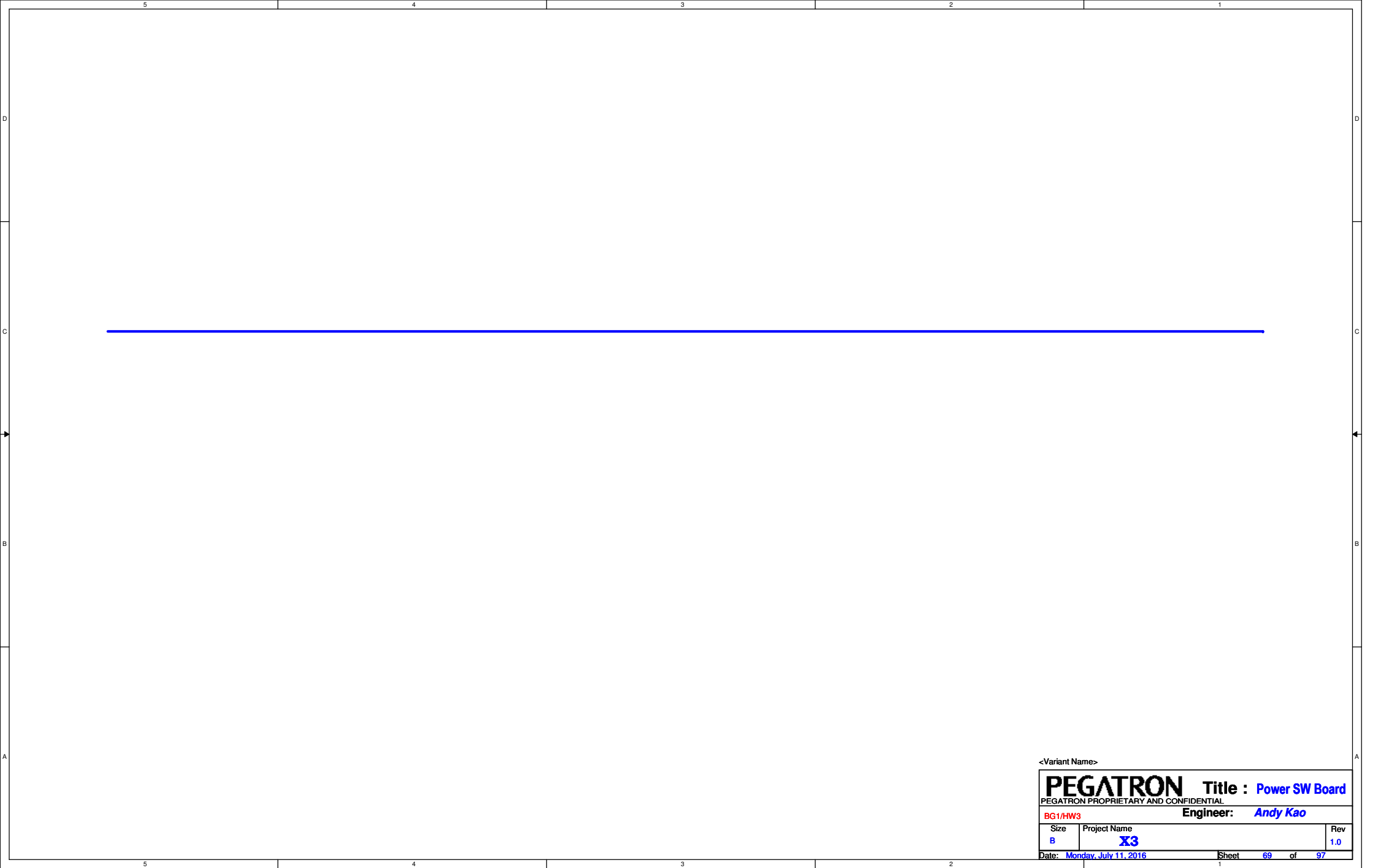
Delay By EC(2ms+ EC processing time (3ms~33ms))



For shut down Sequence
Tplt17 < 1us

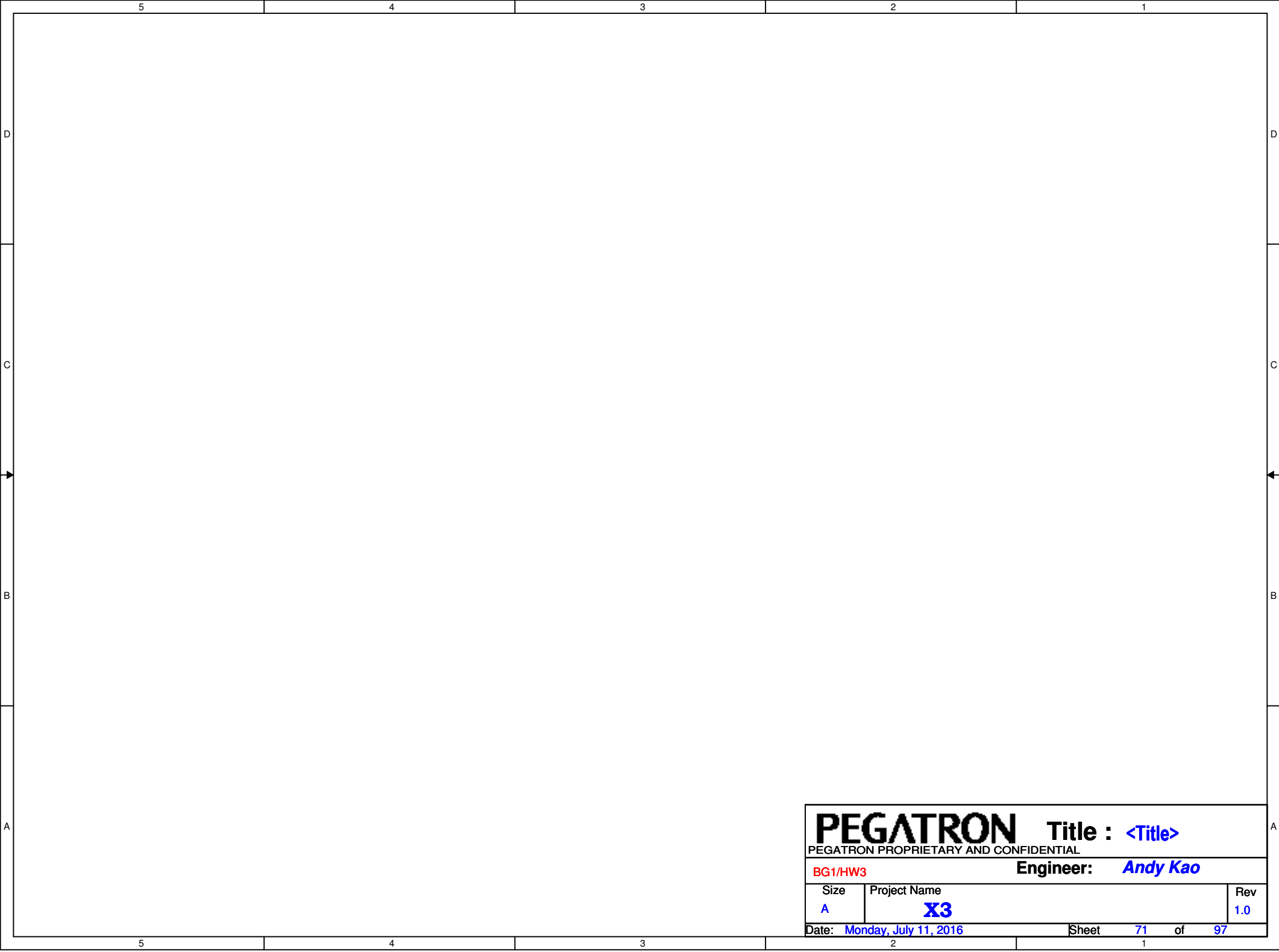


For shut down Sequence Tplt17 < 1us
Due to PDG1.2 Figure 43-5. SYS_PWROK
drop after PM_SUSB# before CPU_VRON
to add this solution

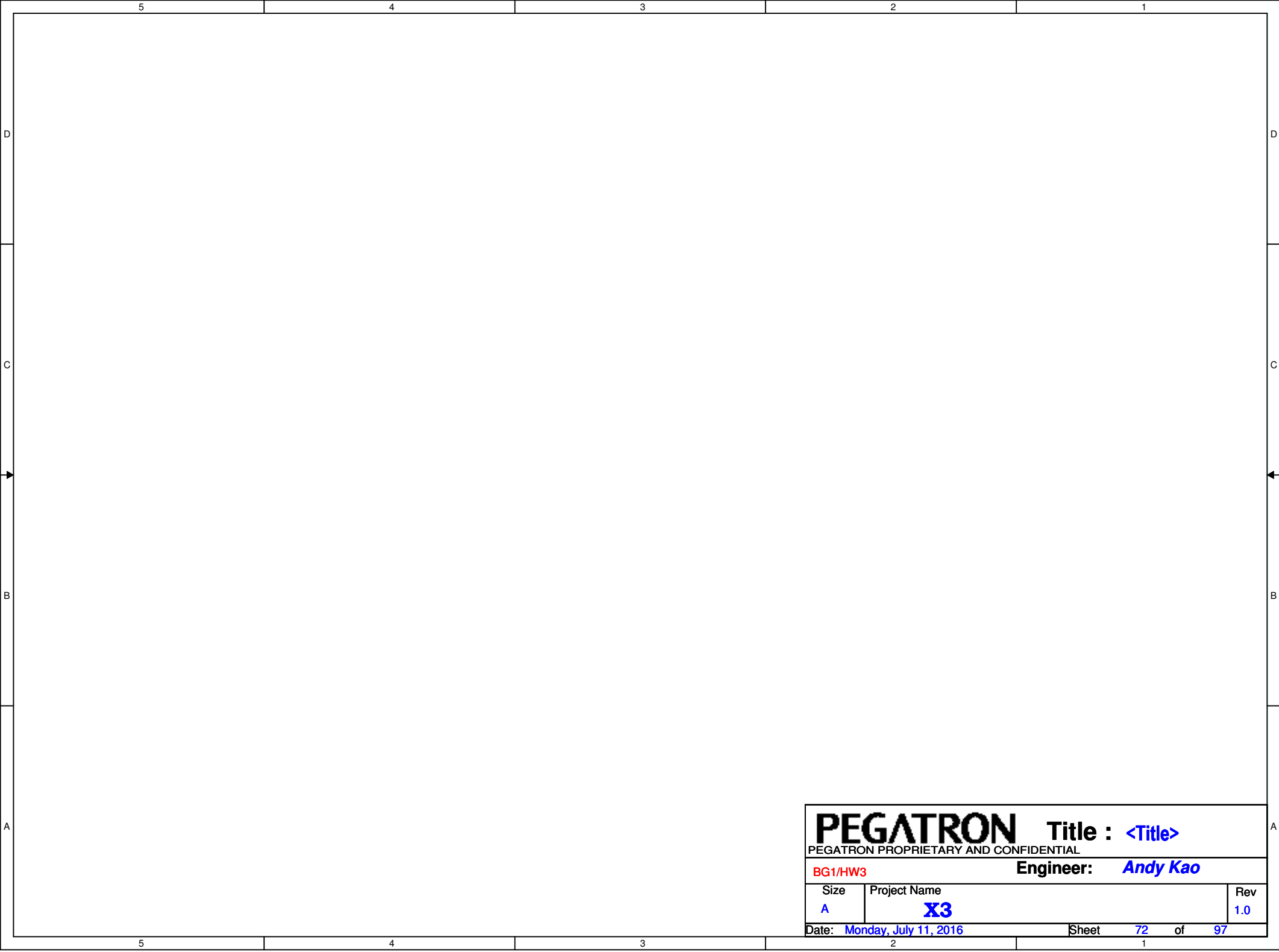


5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

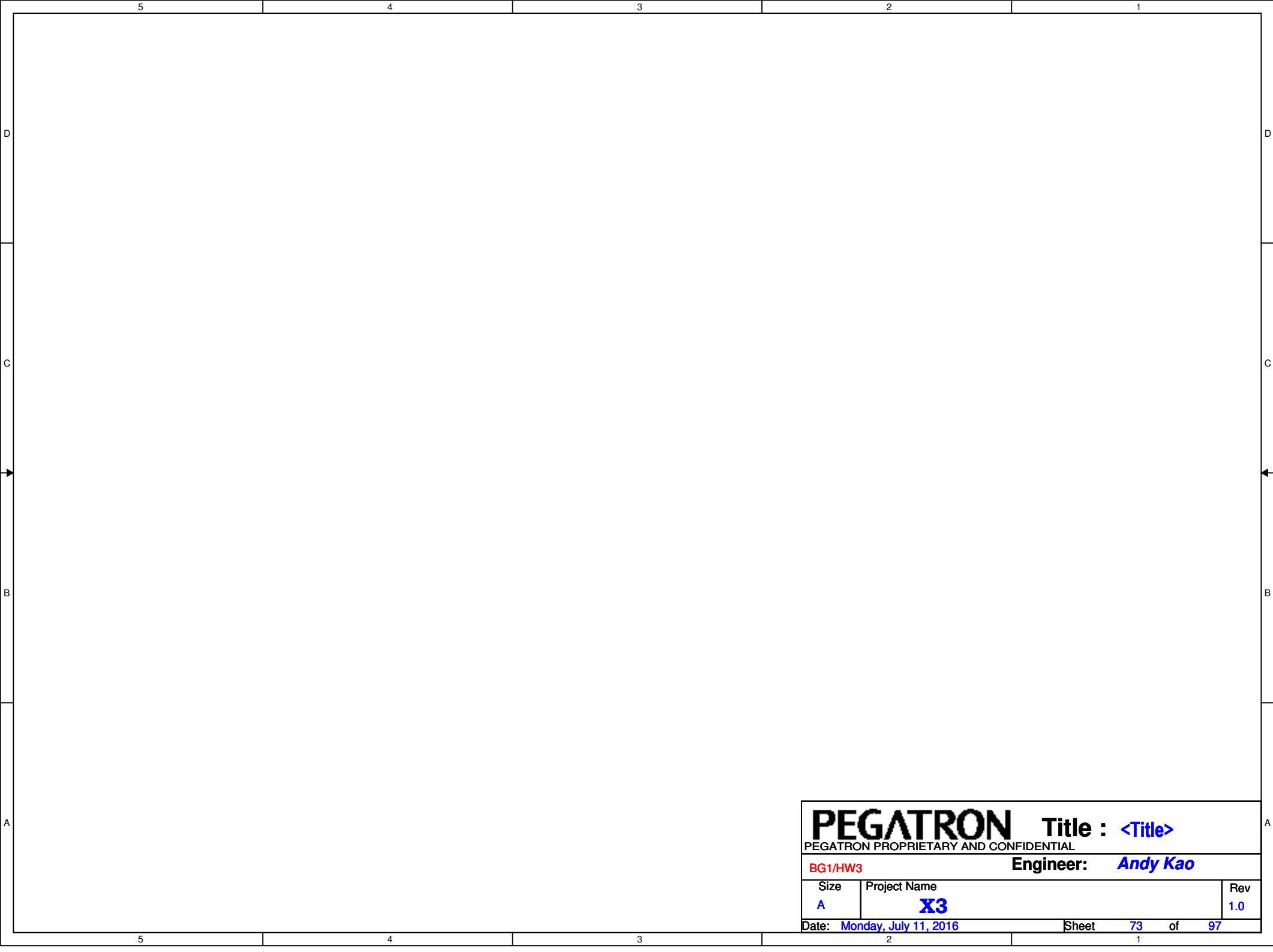
PEGATRON Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: <i>Andy Kao</i>
Size <i>A</i>	Project Name X3	Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>70</i> of <i>97</i>



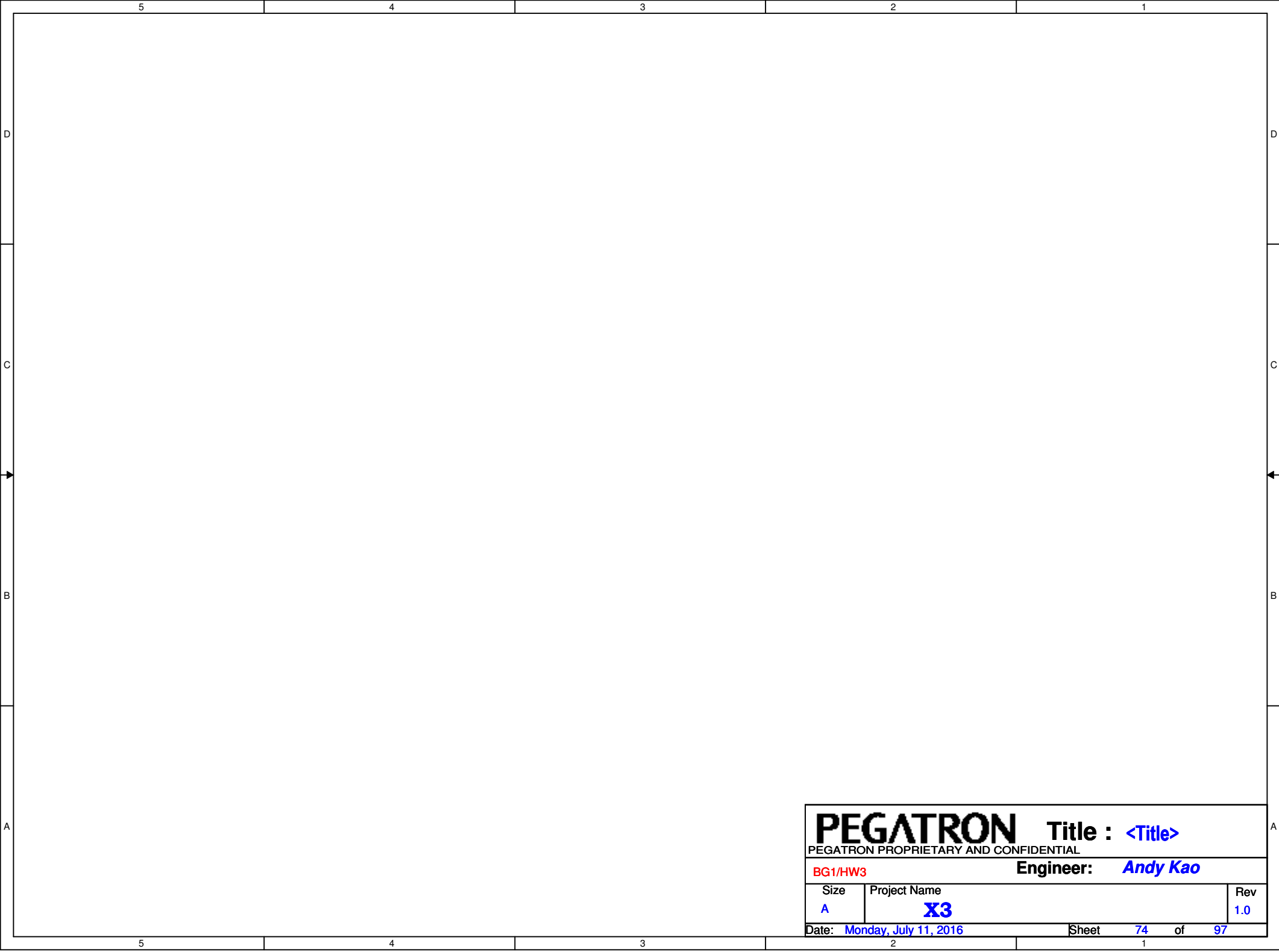
PEGATRON Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: <i>Andy Kao</i>
Size A	Project Name X3	Rev 1.0
Date: Monday, July 11, 2016		Sheet 71 of 97



PEGATRON		Title : <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size	Project Name		Rev
<i>A</i>	<i>X3</i>		<i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>72</i> of <i>97</i>	



PEGATRON Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: <i>Andy Kao</i>
Size <i>A</i>	Project Name X3	Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>73</i> of <i>97</i>



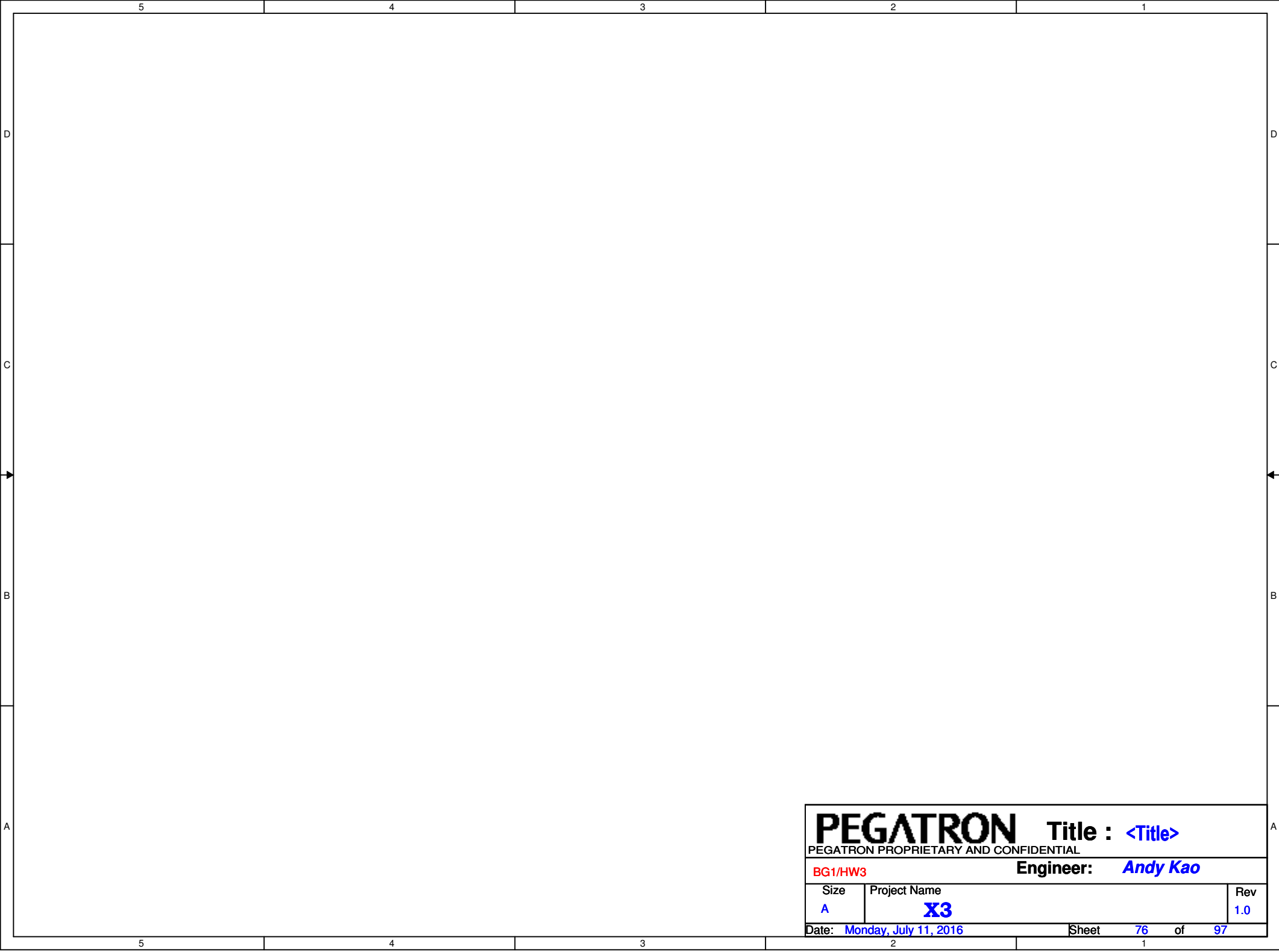
PEGATRON Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: <i>Andy Kao</i>
Size <i>A</i>	Project Name X3	Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>74</i> of <i>97</i>

PEGATRON Title : <Title>

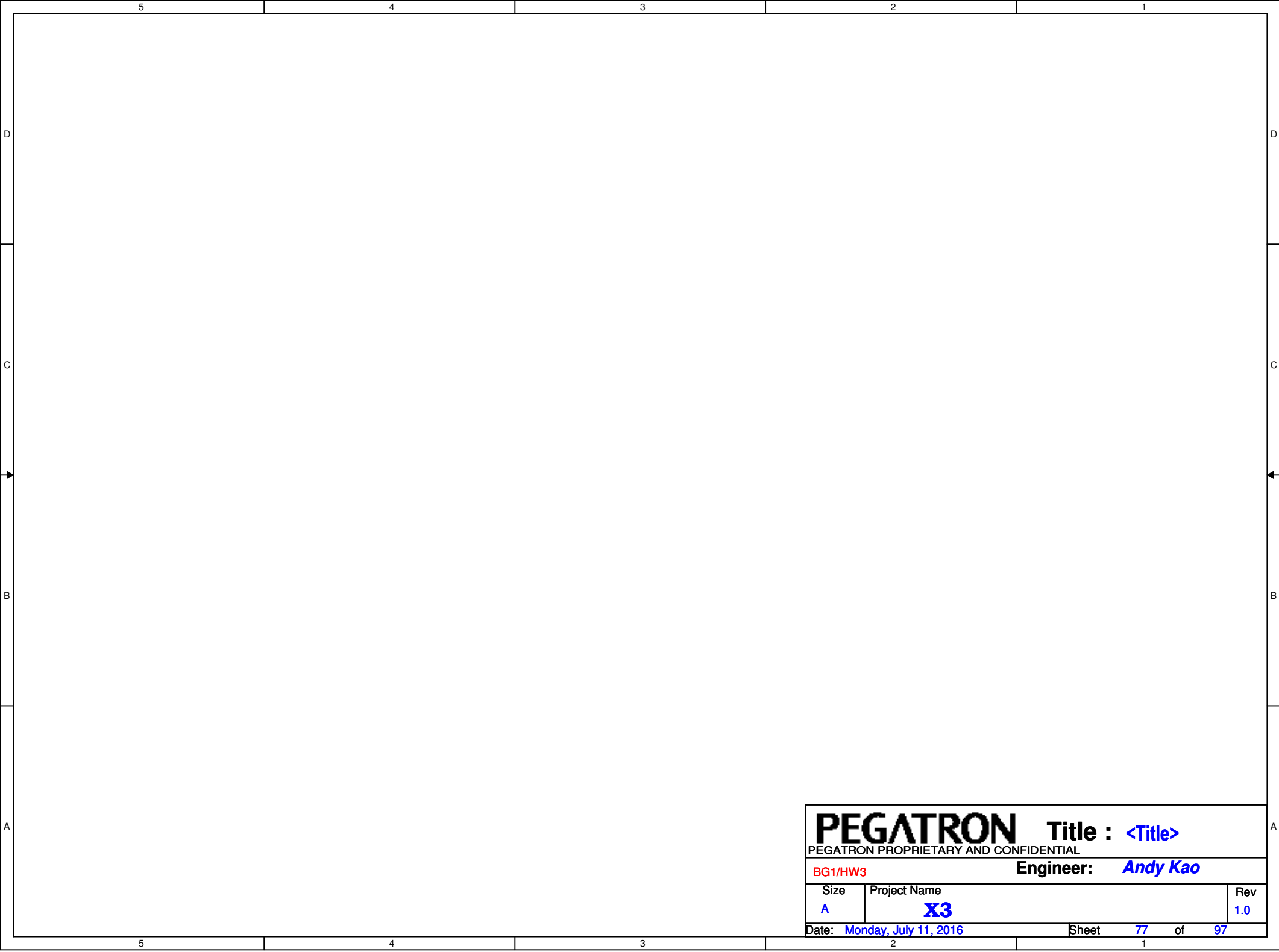
BG1/HW3 **Engineer:** *Andy Kao*

Size A	Project Name X3	Rev 1.0
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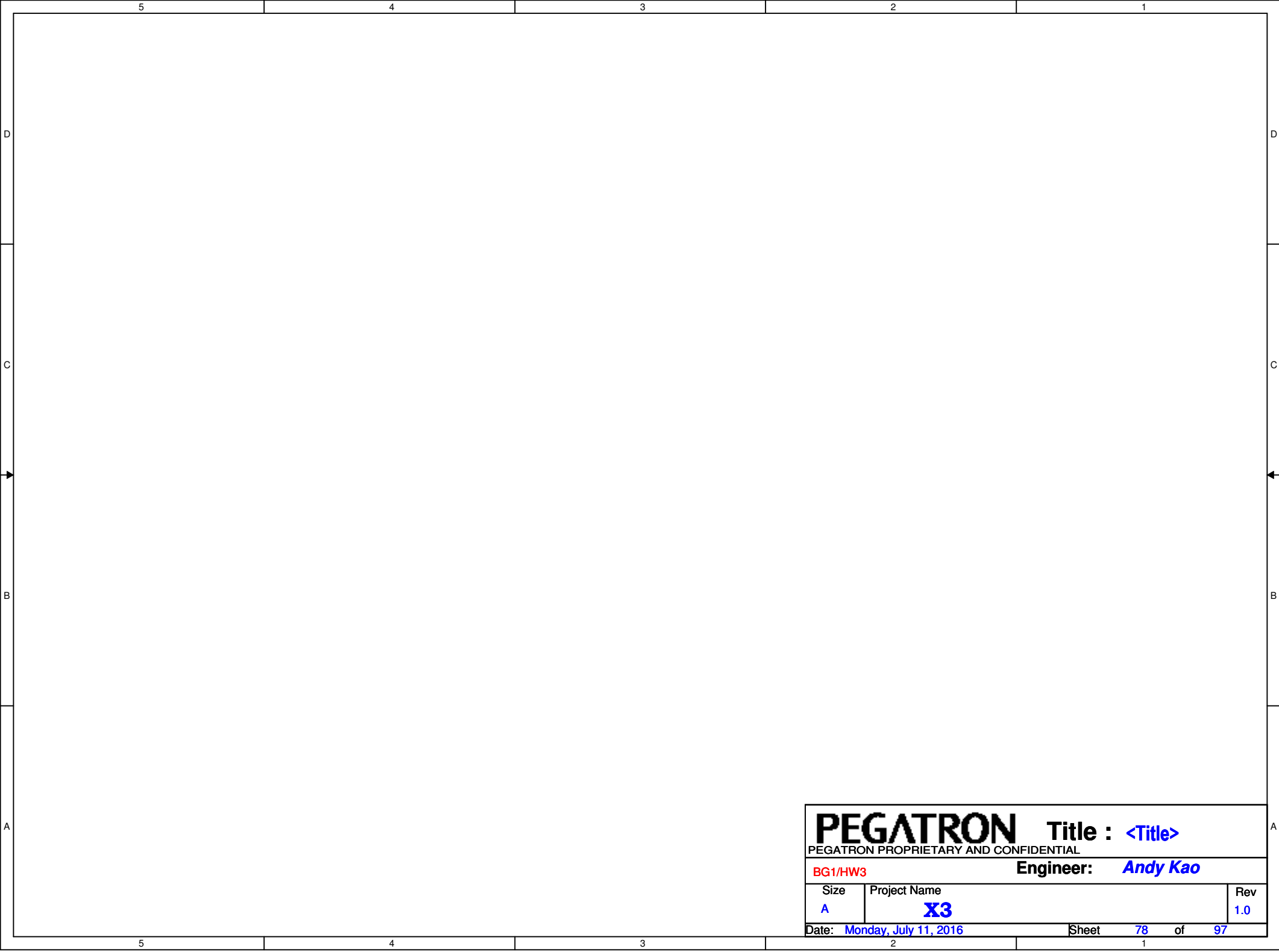
Date: Monday, July 11, 2016	Sheet 75 of 97
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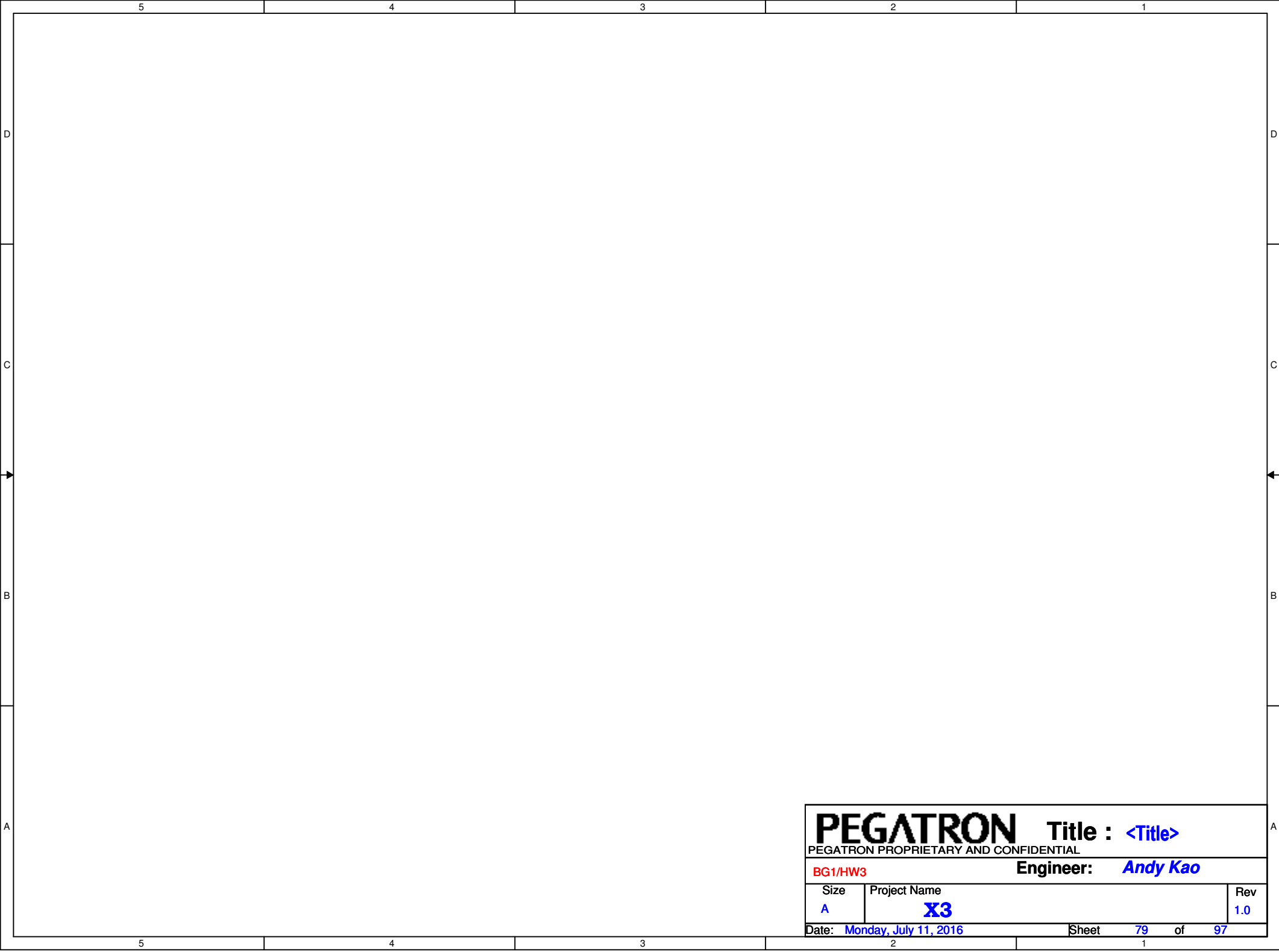
PEGATRON Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: <i>Andy Kao</i>
Size A	Project Name X3	Rev 1.0
Date: Monday, July 11, 2016		Sheet 76 of 97



PEGATRON		Title : <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size	Project Name		Rev
<i>A</i>	<i>X3</i>		<i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>77</i> of <i>97</i>	

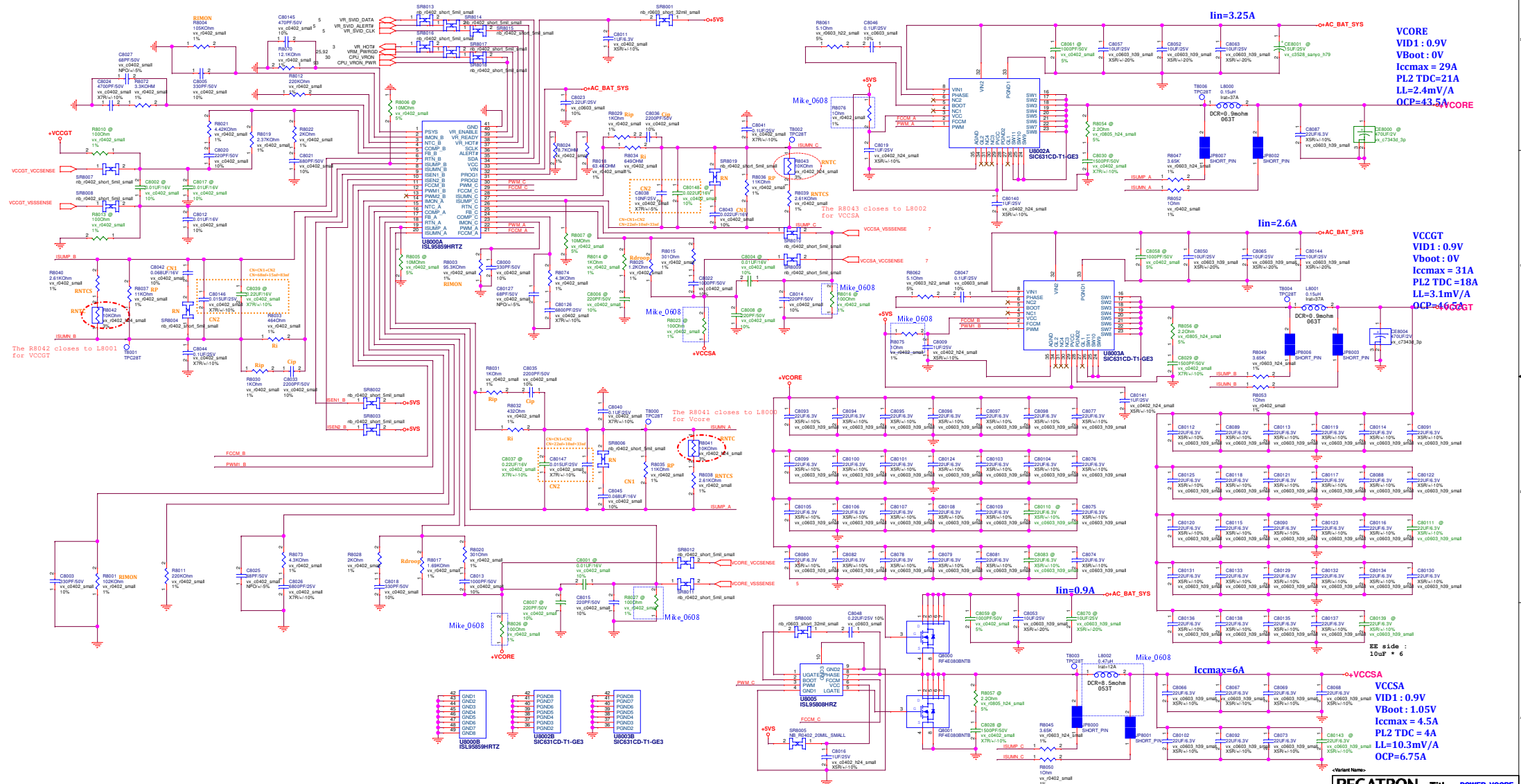


PEGATRON		Title : <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size <i>A</i>	Project Name X3		Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>78</i> of <i>97</i>	

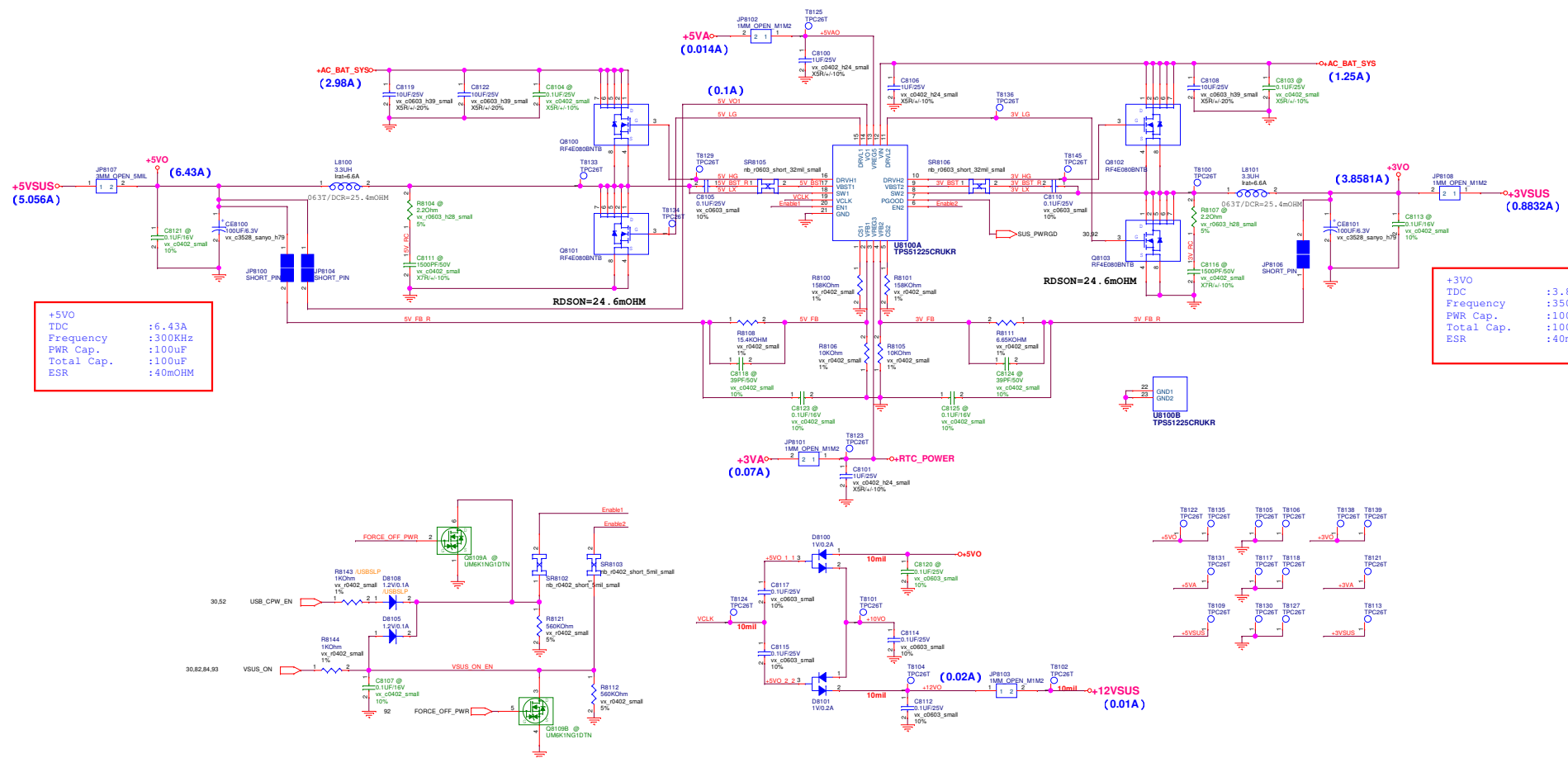


PEGATRON		Title : <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size <i>A</i>	Project Name X3		Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>79</i> of <i>97</i>	

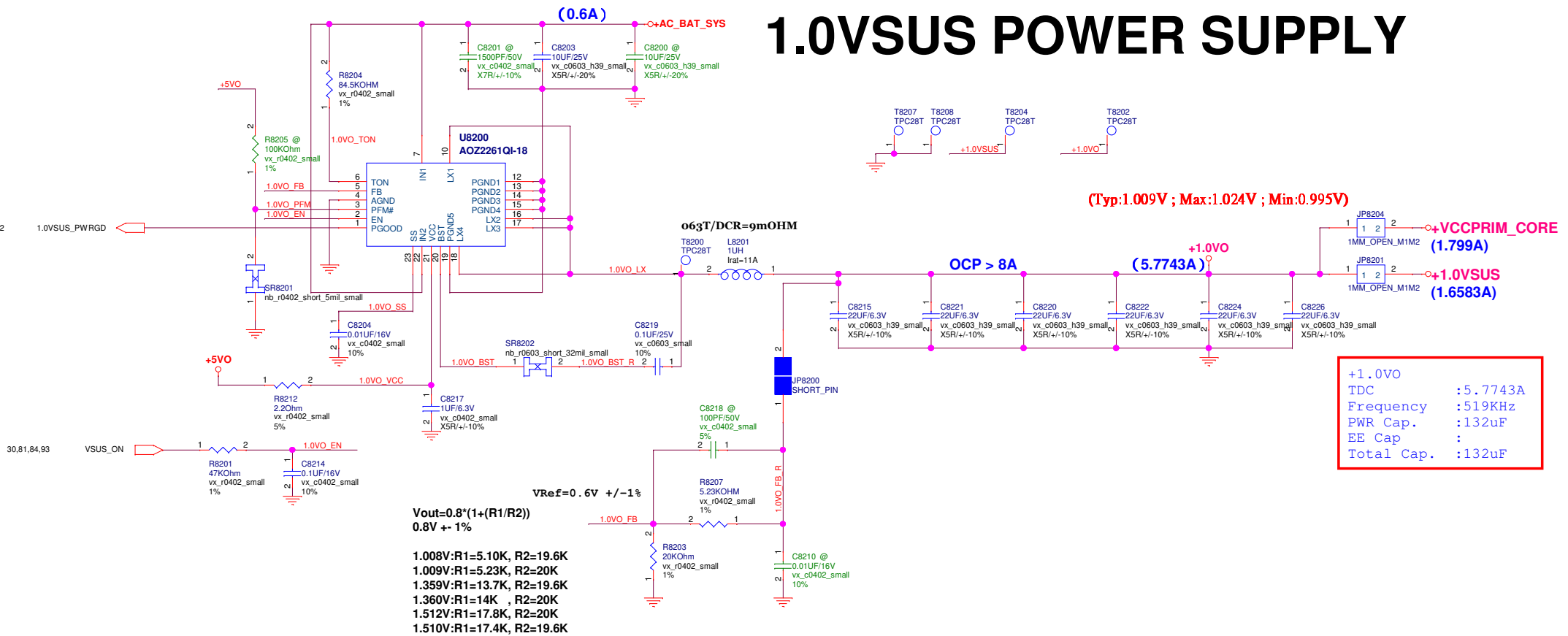
VCORE & VCCGT & VCCSA POWER SUPPLY



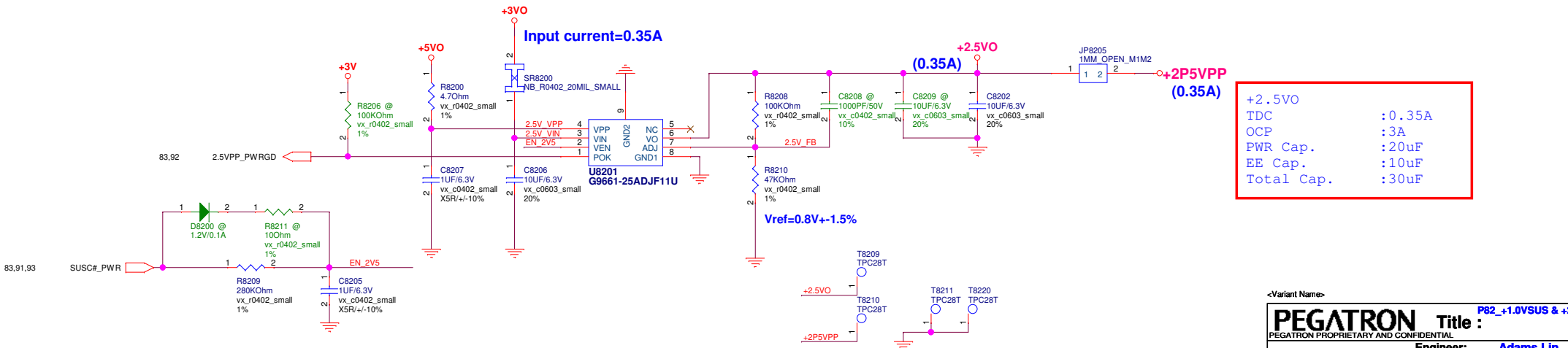
5VO & 3VO POWER SUPPLY



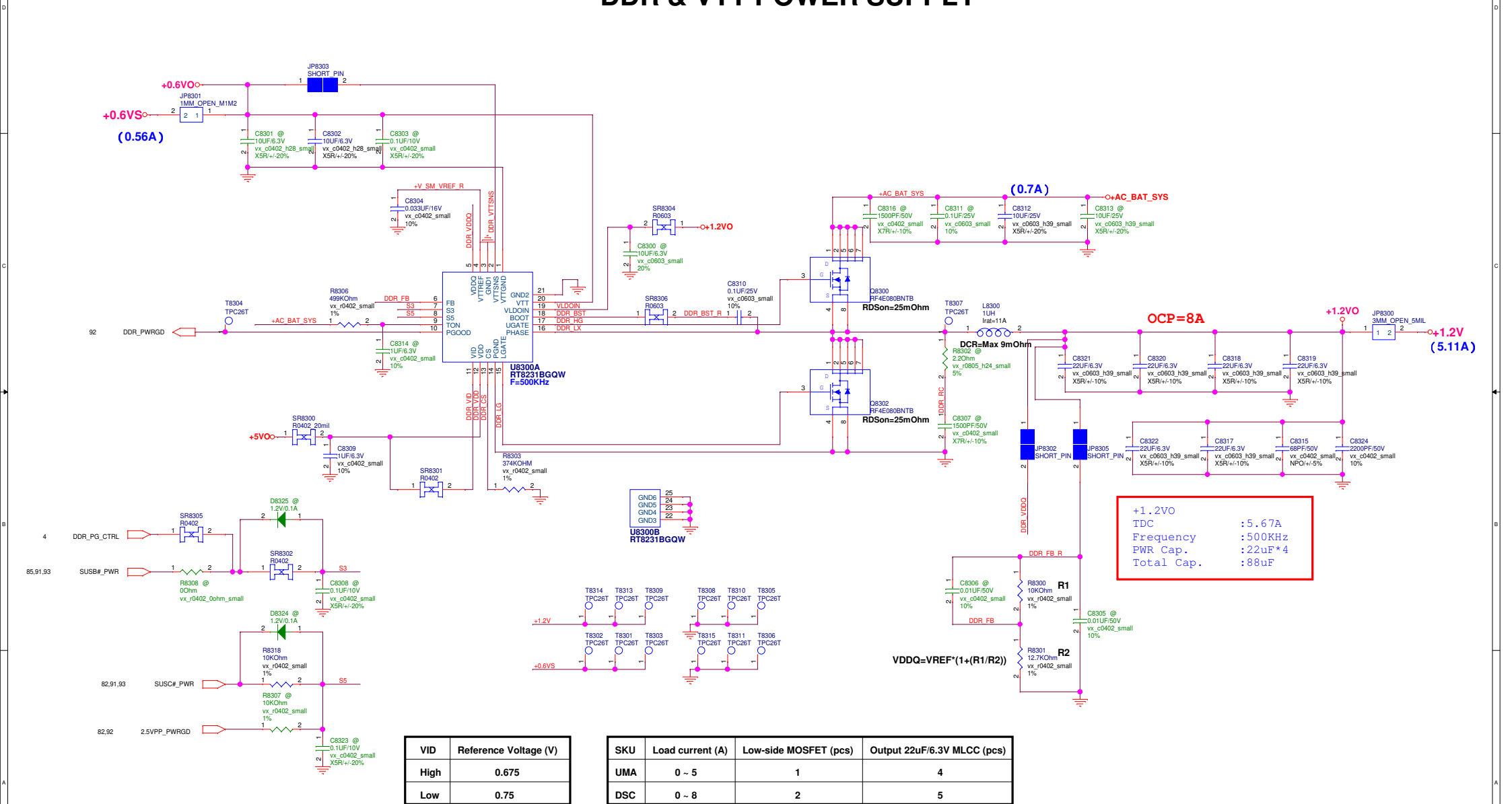
1.0VSUS POWER SUPPLY



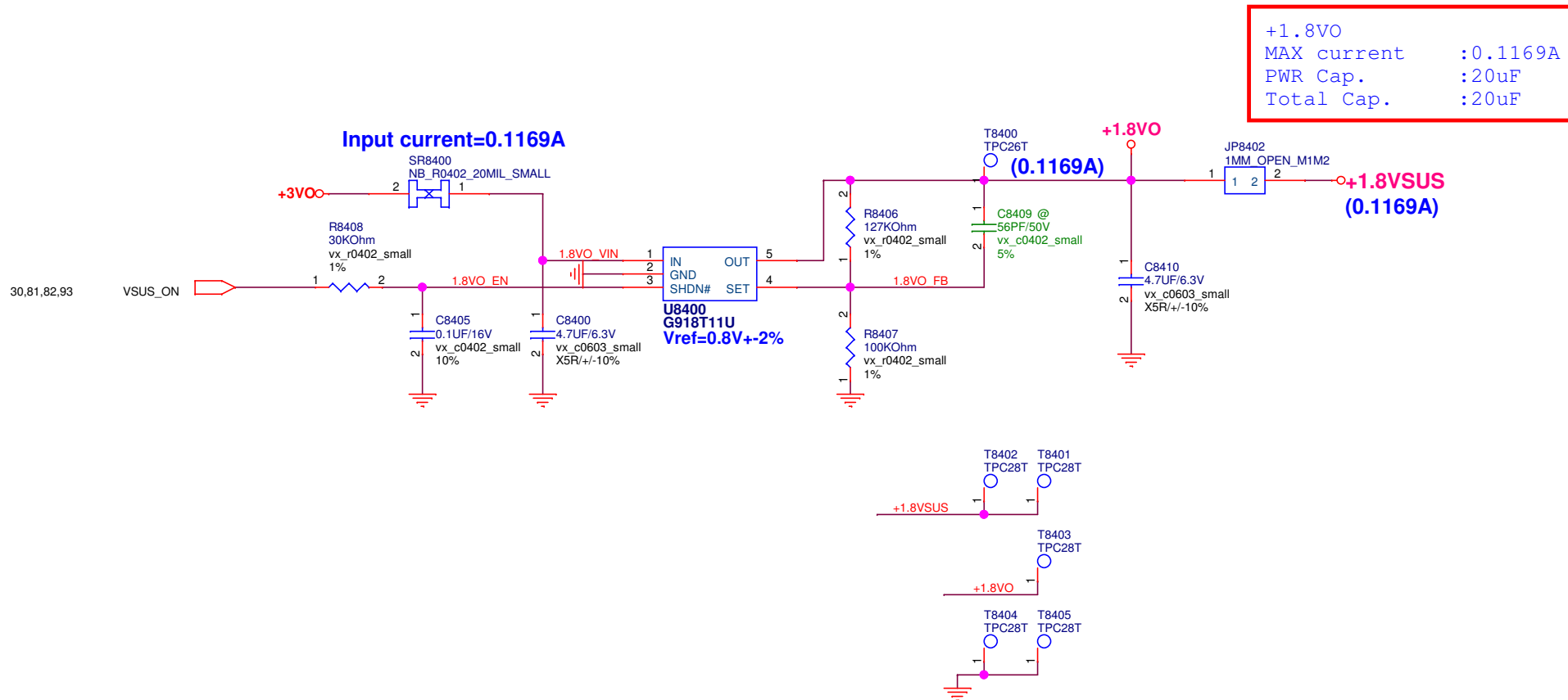
2.5V POWER SUPPLY



DBIT & VHF POWER SUPPLY



1.8VSUS POWER SUPPLY



<Variant Name>

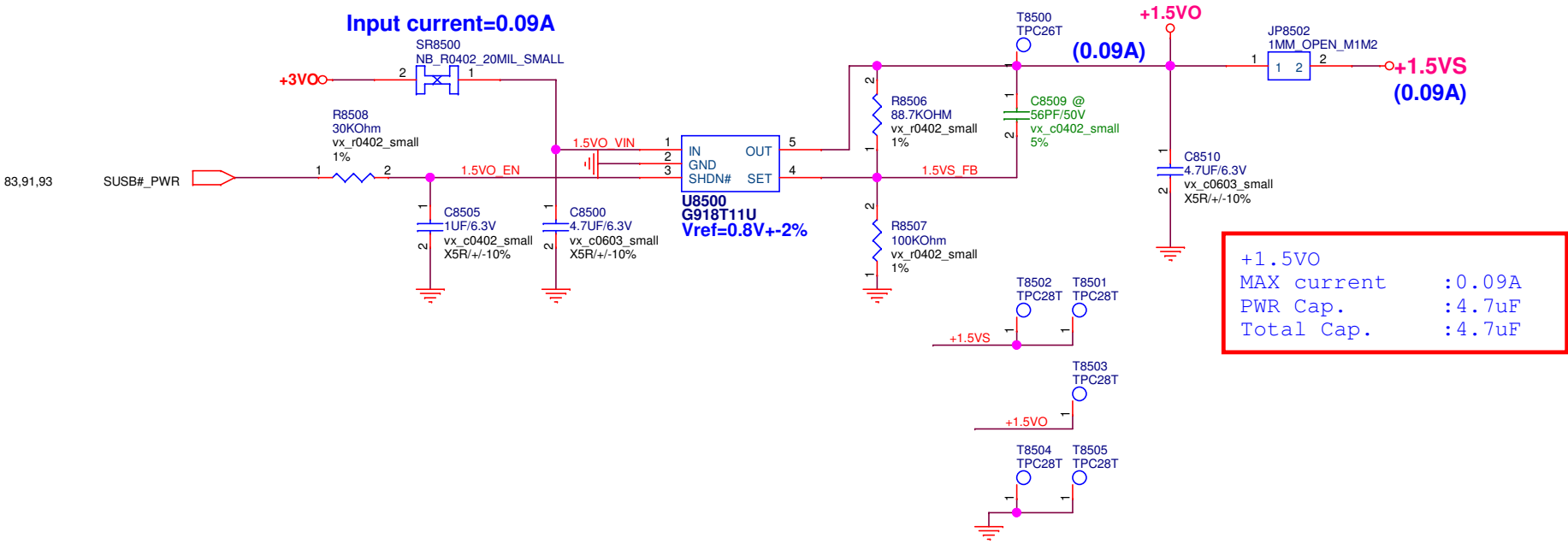
PEGATRON Title : POWER_+1.8VSUS

Engineer: **Adams Lin**

Size Custom	Project Name X3	Rev
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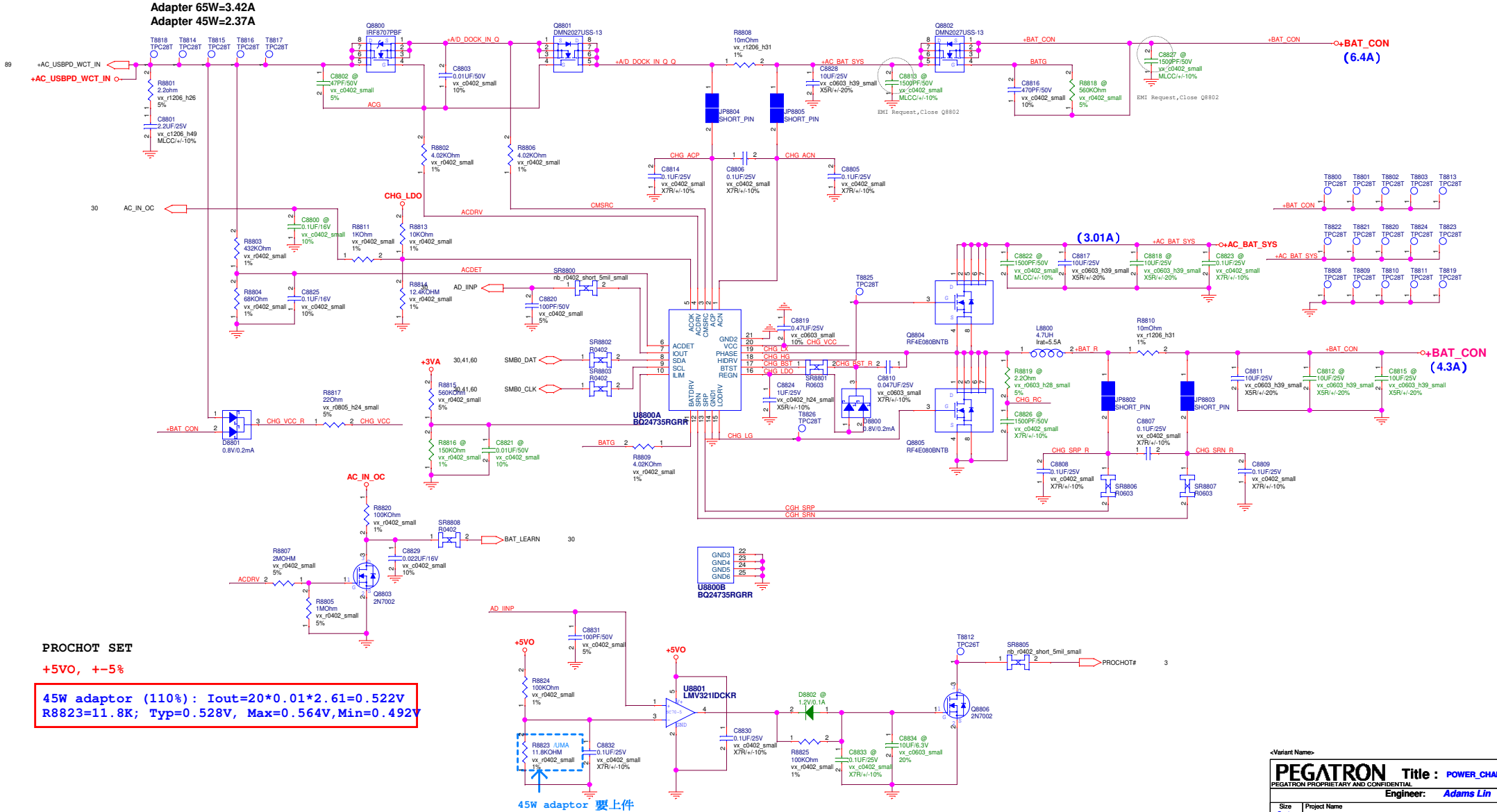
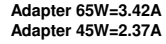
1.5VS POWER SUPPLY



<Variant Name>

PEGATRON		Title : POWER_+1.5VS	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		Engineer: Adams Lin	
Size Custom	Project Name X3		Rev 1.1
Date: Monday, July 11, 2016		Sheet	85 of 94

BATTERY CHARGER



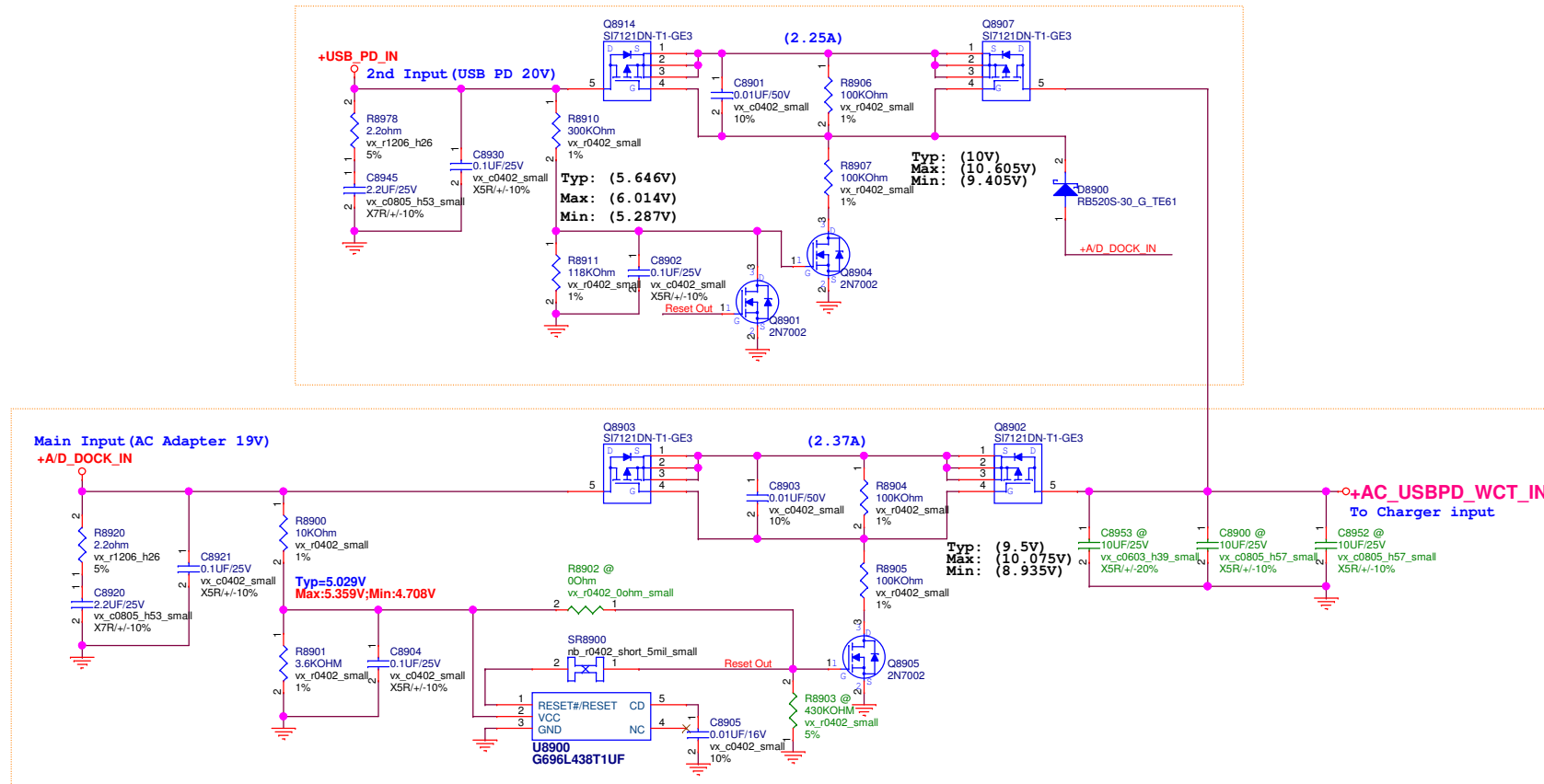
PROCHOT SET

+5V0, +−5%

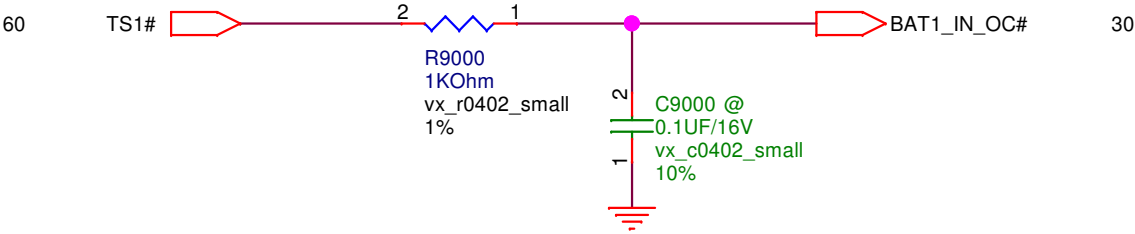
45W adaptor (110%): $I_{out}=20*0.01*2.61=0.522V$
R8823=11.8K; Typ=0.528V, Max=0.564V, Min=0.492V

45W adaptor 要上件

2 Input switch Circuit



BATTERY IN DETECT



<Variant Name>

PEGATRON

Title : POWER_DETECT

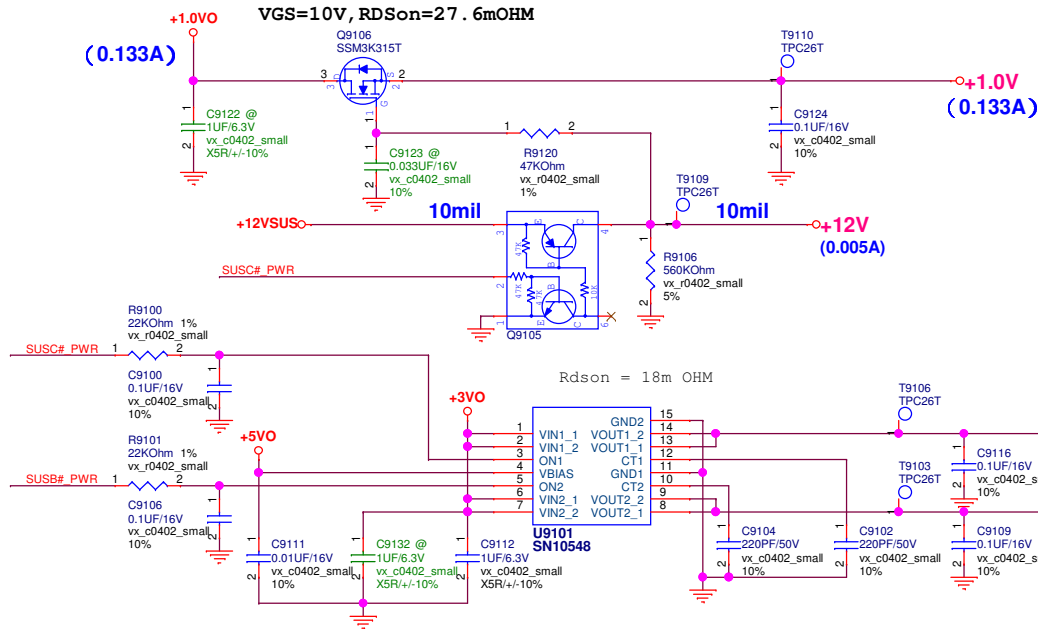
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Adams Lin

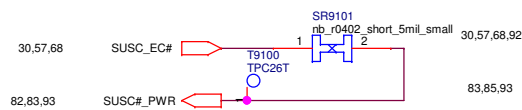
Size Custom	Project Name X3	Rev 1.1
Date: Monday, July 11, 2016	Sheet 90 of 94	

SUSC#_PWR POWER

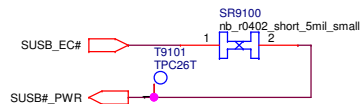
VGS=10V, RDSon=27.6mOHM



SUSC#_PWR POWER Control

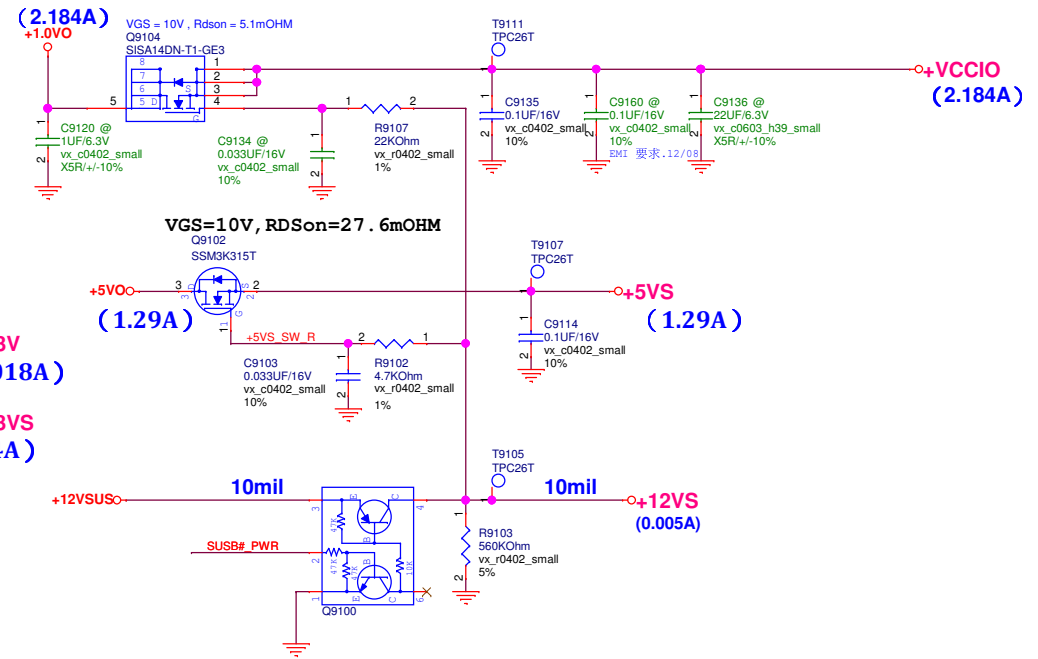


SUSB#_PWR POWER Control



SUSB#_PWR POWER

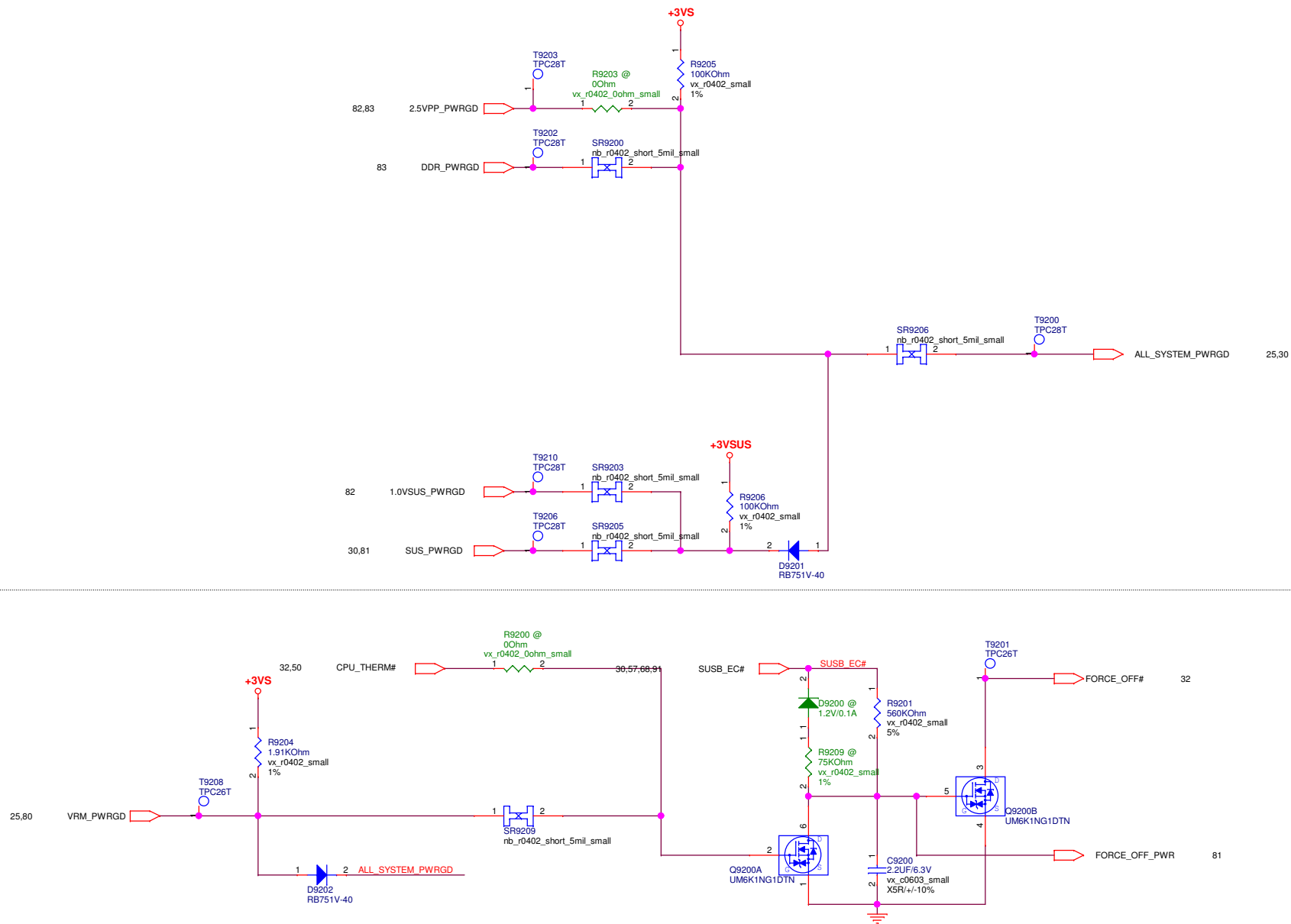
VGS = 10V, RdsOn = 5.1mOHM



<Variant Name>

PEGATRON Title : POWER_LOAD SWITCH			
PEGATRON PROPRIETARY AND CONFIDENTIAL			
Engineer:		Adams Lin	
Size	Project Name	X3	Rev
Custom			1.1
Date:	Monday, July 11, 2016	Sheet	91 of 94

POWER GOOD DETECTOR

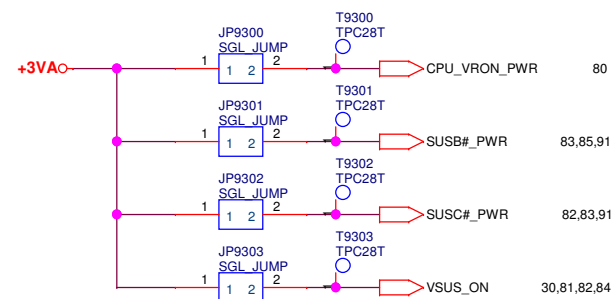


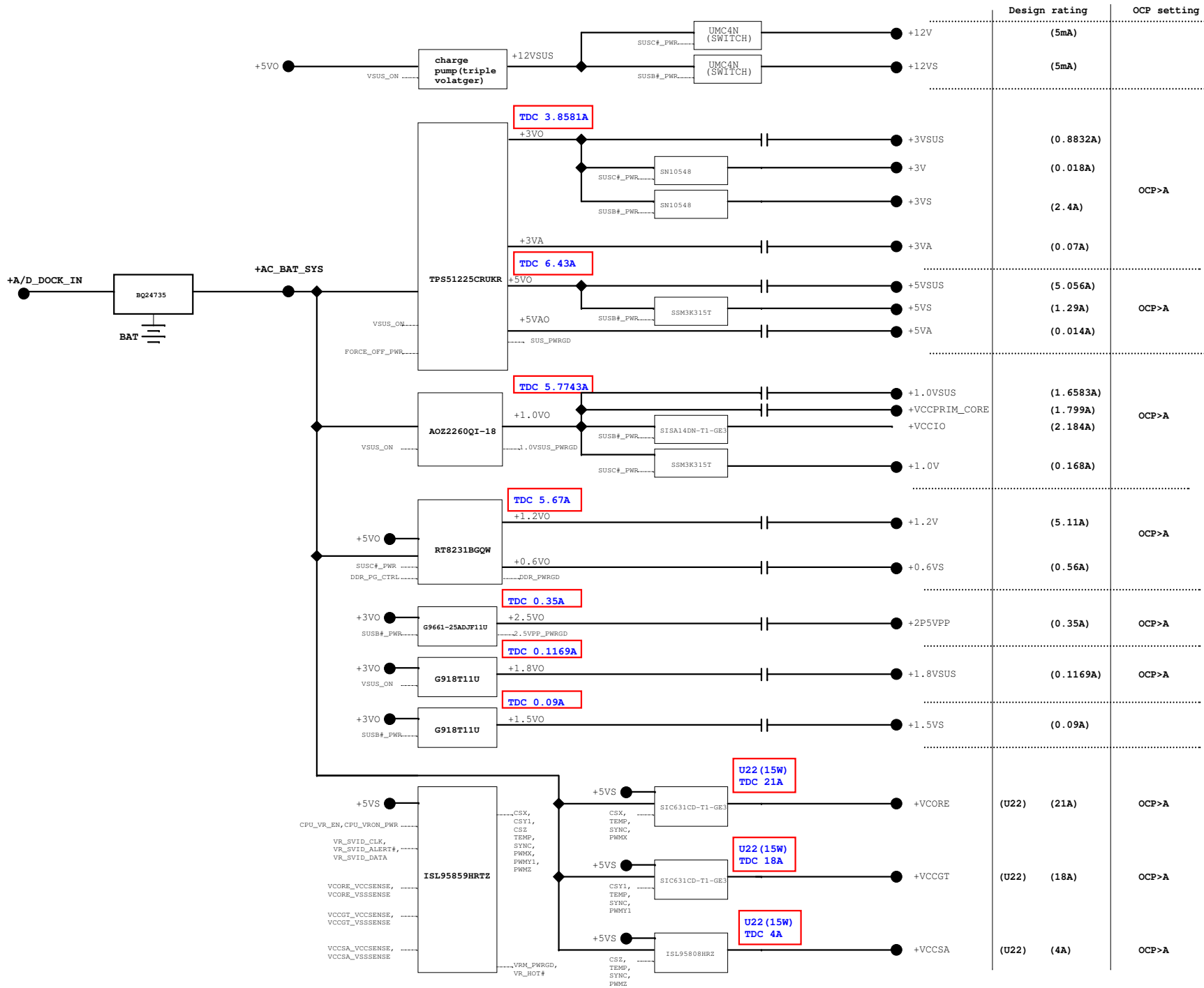
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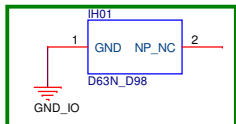
PEGATRON		Title : POWER_PROTECT	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		Engineer: Adams Lin	
Size Custom	Project Name X3	Rev 1.1	
Date: Monday, July 11, 2016	Sheet 92 of 94		

+USB_PD_IN	→	+USB_PD_IN	42,89
+A/D_DOCK_IN	→	+A/D_DOCK_IN	60,89
+AC_USBDPD_WCT_IN	→	+AC_USBDPD_WCT_IN	88,89
+AC_BAT_SYS	→	+AC_BAT_SYS	43,45,80,81,82,83,88
+BAT_CON	→	+BAT_CON	60,88
+RTC_POWER	→	+RTC_POWER	81
+5VA	→	+5VA	31,56,81
+3VA	→	+3VA	24,30,31,36,41,43,53,57,64,81,88
+5VO	→	+5VO	26,81,82,83,88,91
+3VO	→	+3VO	81,82,84,85,91
+2.5VO	→	+2.5VO	82
+1.8VO	→	+1.8VO	84
+1.2VO	→	+1.2VO	83
+1.0VO	→	+1.0VO	82,91
+0.6VO	→	+0.6VO	83
+12VSUS	→	+12VSUS	28,81,91
+5VSUS	→	+5VSUS	41,42,52,56,64,81
+3VSUS	→	+3VSUS	4,24,25,26,28,30,31,41,42,51,53,62,64,68,81,92
+1.8VSUS	→	+1.8VSUS	9,21,22,26,84
+1.0VSUS	→	+1.0VSUS	26,82
+12V	→	+12V	57,91
+2P5VPP	→	+2P5VPP	16,17,57,82
+1.2V	→	+1.2V	4,7,15,16,17,19,57,83
+1.0V	→	+1.0V	7,57,91
+12VS	→	+12VS	31,48,57,91
+5VS	→	+5VS	31,36,45,48,50,51,57,80,91
+3VS	→	+3VS	3,4,21,22,23,24,30,31,32,36,37,44,45,47,50,51,53,57,62,64,91,92
+0.6VS	→	+0.6VS	15,57,83
+VCORE	→	+VCORE	5,80
+VCCGT	→	+VCCGT	6,80
+VCCSA	→	+VCCSA	7,80
+VCCIO	→	+VCCIO	3,7,9,57,91
+VCCPRIM_CORE	→	+VCCPRIM_CORE	26,82

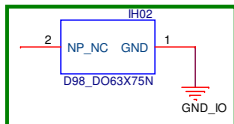
FOR POWER TEST





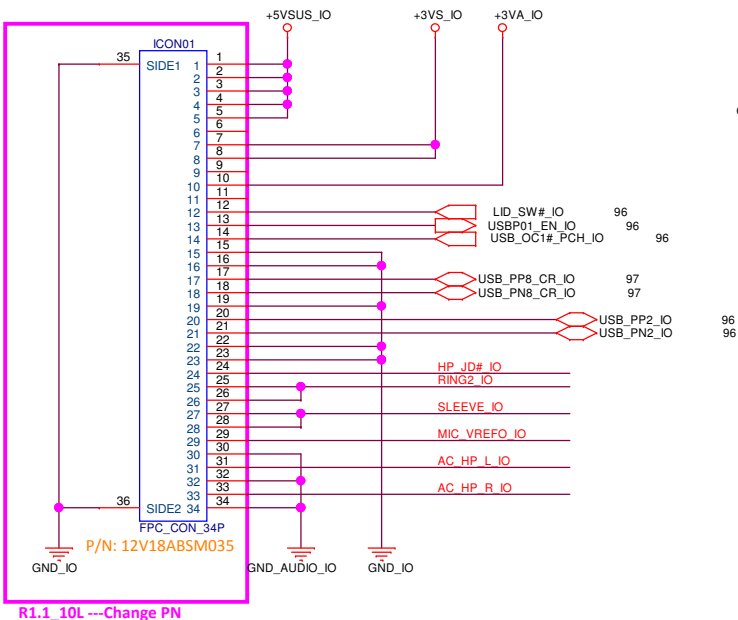
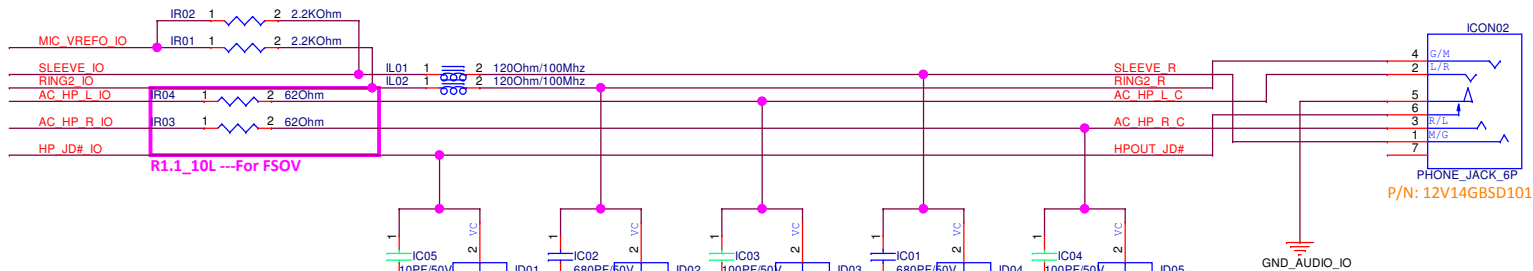


2016.6.6 R1.2_10L ---For ME

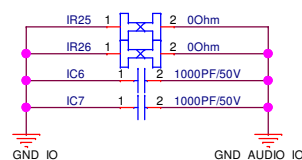


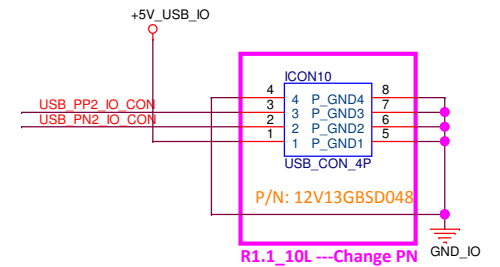
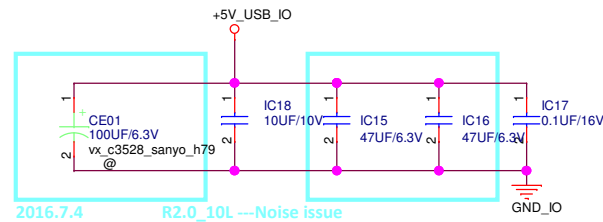
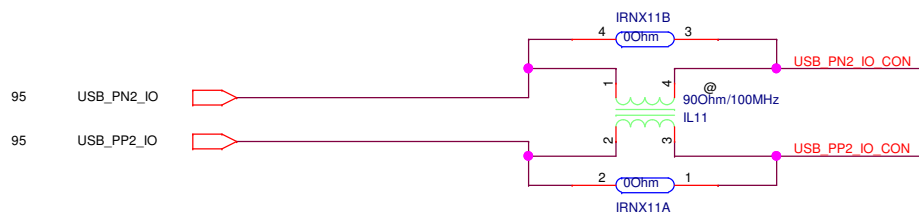
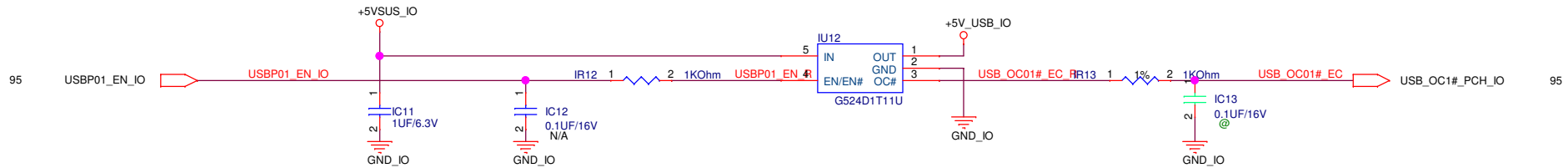
2016.6.6 R1.2_10L ---For ME

AUDIO JACK

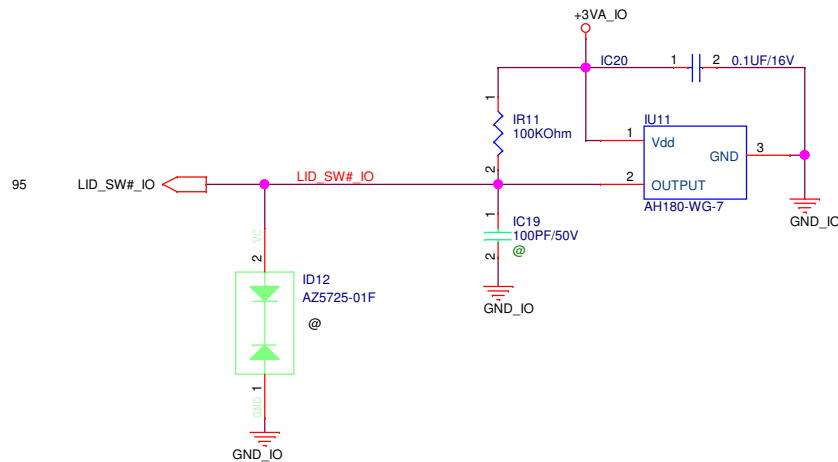
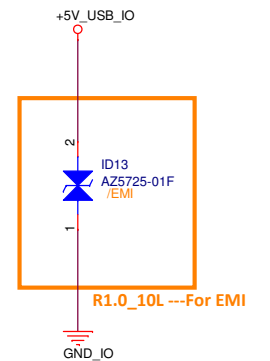
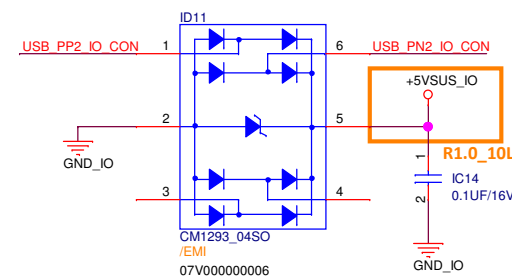


R1.1_10L ---Change PN

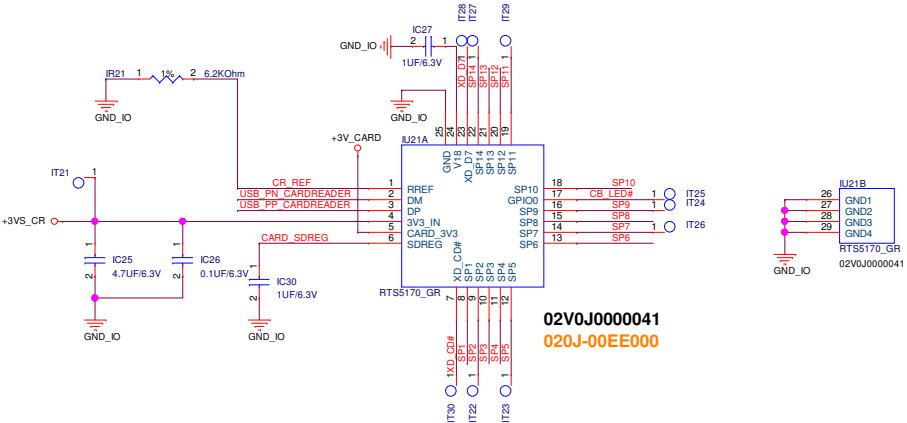
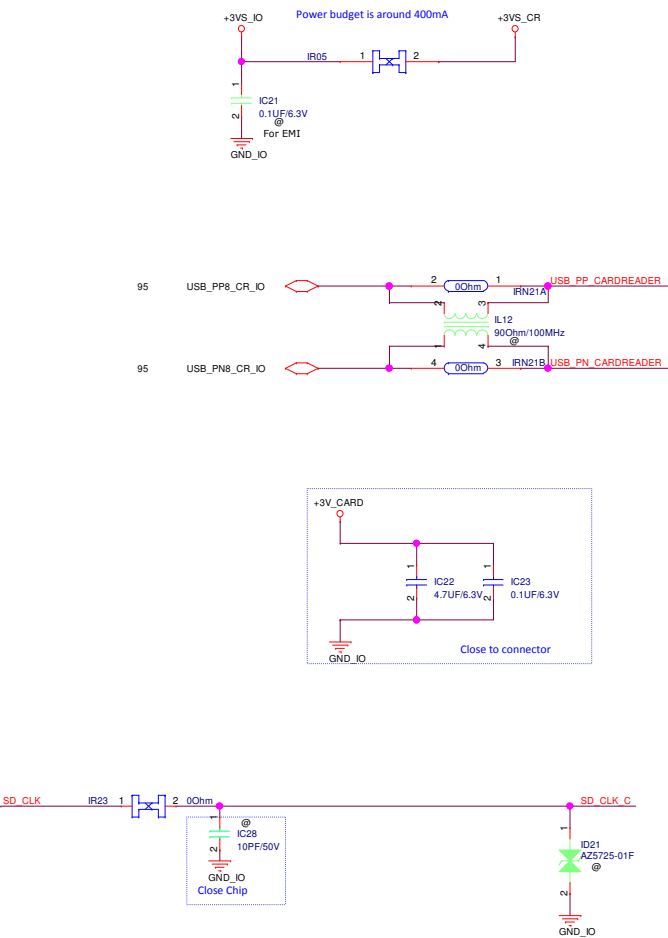




PLACE ESD Diodes near USB Connector



Cardreader



02V0J0000041
020J-00EE000

RTSS170-GR Share Pin Assignment

SP1	SD W/P
SP3	SD D1
SP4	SD D0
SP6	SD C/D#
SP8	SD CLK
SP10	SD CMD
SP12	SD D3
SP13	SD D2

